Stability Analysis of PWM Converters Connected to General Load Subsystems

Syam Kumar Pidaparthy and Byungcho Choi
School of Electronics Engineering
Kyungpook National University, Daegu, South Korea
bchoi@ee.knu.ac.kr

***Abstract*— This paper investigates stability of dc-to-dc converters deriving another dc-to-dc converter through a filter stage. The impacts of the downstream filter/converter stage on the absolute and relative stabilities of the upstream converter are analyzed. The absolute stability is examined using the minor loop gain, defined as the ratio of the impedances seen at the output port of the upstream converter. The relative stability is assessed using the loop gain expression of the upstream converter. This paper reveals that the downstream filter/converter stage rarely destabilizes the upstream converter, but usually dictates the loop gain characteristics of the upstream converter and frequently determines the phase margin and 0 dB crossover frequency of the loop gain. This paper proposes a simple method to determine the stability margins of the converter from the minor loop gain. The theoretical predictions are supported by both small-signal simulations and experimental measurements.**

Index Terms*— Cascaded converters, Dc-to-dc power conversion systems, filter stage, load impedance, loop gain analysis, minor loop gain, stability analysis.

I. Introduction

Dc-to-dc power conversion systems often employ cascaded stages of dc-to-dc converters for an efficient and reliable power conversion [1]–[4]. For these multi-stage power systems, a filter stage is usually placed between the converter stages, in order to prevent the pulsating input currents of the converters from circulating through the system, thereby complying with EMI standards [3], [5]. Figure 1 shows an example of such dc-to-dc power conversion systems. The front-end converter interfaces with the voltage source and provides an intermediate dc output. The intermediate dc voltage is fed to the load converter via a single-stage filter. The load converter then produces a tightly regulated dc voltage for the load [1], [2], [5], [6].

The two-stage dc-to-dc power conversion system in Fig. 1 is viewed as a connection of the two functional stages. The front-end converter is considered as the upstream converter stage and the combination of the filter stage and load converter is treated as the load subsystem. The upstream converter can be designed and tested as a standalone converter stage feeding a current sink load [7], [8] This approach enables us to perform the control design based on the dc current requirement of the converter without any prior information about the dynamics of the load subsystem. The loop gain can be designed for the stability and performance of the standalone front-end converter. However, when the front-end converter is integrated with the load subsystem, the converter's loop gain will be affected and the stability of the integrated converter needs to be reevaluated from the modified loop gain characteristics [9], [10].

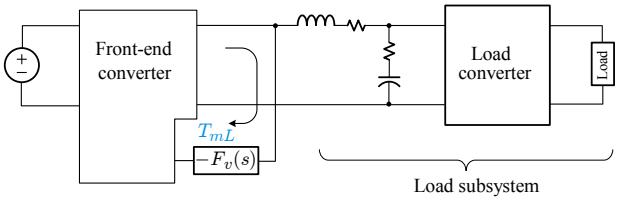


Fig. 1. Two stage dc-to-dc power conversion system. The functional block $F_v(s)$ represents the feedback compensation of the front-end converter. The load converter is also closed-loop controlled.

This paper deals with the stability analysis of dc-to-dc converters deriving another converter through a filter stage. Although the two-stage power conversion system in Fig. 1 is used as an illustrative example, the outcomes of this paper can be extended to include other dc-to-dc converters employed in general dc-to-dc power conversion systems. The theoretical predictions are validated with both small-signal simulations and experimental measurements using a prototype two-stage power conversion system.

This paper first investigates the absolute stability of the upstream converter. The method of the minor loop gain [4], [11]–[13] is adapted for this study, which utilizes the ratio of the two impedances at the interface of the subsystems as a means of stability assessment. This part addresses the possibility/risk of destabilizing the upstream converter by integrating with certain load subsystems which are built following the standard design procedures [6], [14], [15].

The latter part of the paper analyzes the relative stability of the upstream converter. The impacts of the load subsystem [6], [16] on the loop gain of the upstream converter are examined. The asymptotic Bode plot method [14], [15], [17] is applied to the loop gain expression of the upstream converter. This paper shows that the minor loop gain, used for the absolute stability analysis, also carries the information about relative stability of the upstream converter. This paper reveals that the load subsystem rarely destabilizes the upstream converter, but usually governs the loop gain characteristics of the converter. In particular, the phase margin and 0 dB crossover frequency of the upstream converter are determined by the minor loop gain. This paper presents a practical method to determine the criteria for the absolute and relative stabilities of the converter from the minor loop gain.

This research was supported by the MSIP (Ministry of Science, ICT & Future Planning), Korea, under the C-ITRC (Convergence Information Technology Research Center) support program (NIPA-2014-H0401-14-1004) supervised by the NIPA (National IT Industry Promotion Agency).

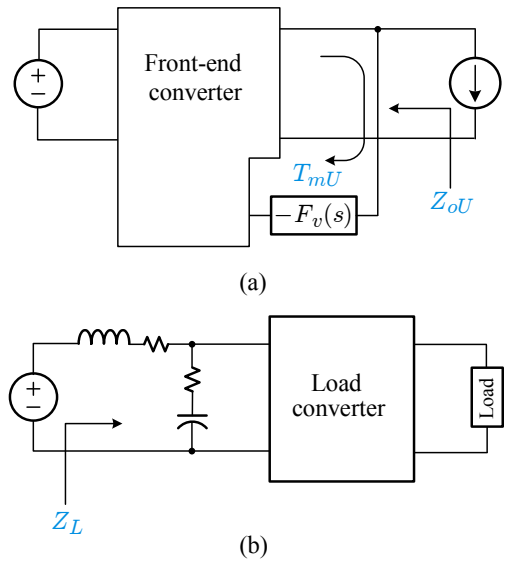


Fig. 2. Illustration of T_{mU}, Z_{oU}, and $Z_L(s)$. (a) Standalone front-end converter. (b) Load subsystem.

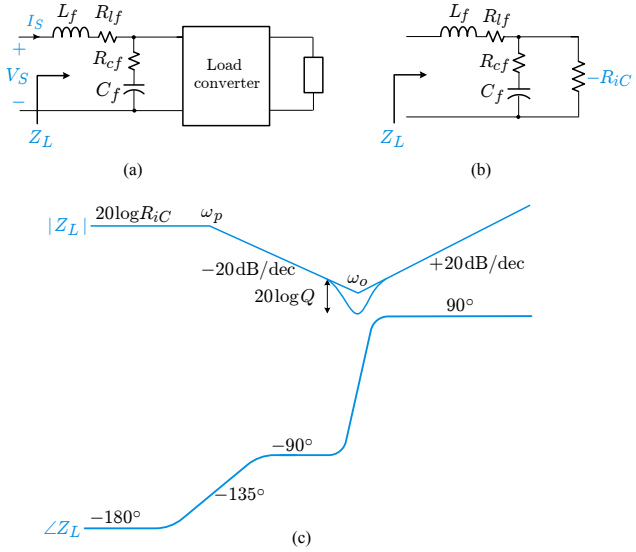


Fig. 3. Load impedance evaluation. (a) Load subsystem. (b) Circuit model. (c) Asymptotic plots for Z_L.

II. Minor Loop Gain and Absolute Stability

This section examines the absolute stability of the front-end converter integrated with the load subsystem. First, the loop gain expression of the integrated converter is introduced and the concept of the minor loop gain is reviewed. Second, the polar plot of the minor loop gain is discussed. Then, the absolute stability of the integrated front-end converter is analyzed by applying the Nyquist stability criterion to the minor loop gain. The possibility or risk of instability due to the integration with the load subsystem is addressed.

A. Loop Gain Expression and Minor Loop Gain

The vital information for the stability analysis of the integrated converter is its loop gain expression. The previous publications [6], [7], [9], [16] showed that the loop gain of the integrated front-end converter, $T_{mL}(s)$ in Fig. 1, is given by

$$T_{mL}(s) = \frac{T_{mU}}{1 + \left(1 + T_{mU}\right)\dfrac{Z_{oU}}{Z_L(s)}} \tag{1}$$

where T_{mU} is the loop gain of the standalone converter terminated with a current sink load and Z_{oU} is the output impedance of the standalone converter. The subscript $_U$ in T_{mU} and Z_{oU} signifies the converter is *unloaded* in the small-signal sense. The $Z_L(s)$ is the input impedance of the load subsystem operating from an ideal voltage source. The impedance $Z_L(s)$ will be referred to as the load impedance in forthcoming discussions. The pictorial illustrations of T_{mU}, Z_{oU}, and $Z_L(s)$ are given in Fig. 2.

Stability of the integrated converter is assessed using the characteristic equation

$$1 + T_{mL}(s) = 1 + \frac{T_{mU}}{1 + \left(1 + T_{mU}\right)\dfrac{Z_{oU}}{Z_L(s)}} = 0 \tag{2}$$

which is rearranged as

$$\left(1 + T_{mU}\right)\left(1 + \frac{Z_{oU}}{Z_L(s)}\right) = 0 \tag{3}$$

The solutions of this equation constitute the poles of the integrated converter. The expression (3) indicates that the poles of the integrated converter are given by the union of the poles of the standalone converter and the solutions of $1 + Z_{oU}/Z_L(s) = 0$. It also reveals that the load impedance does not alter the existing poles of the standalone converter, but creates new poles. We assume the standalone converter is stable. Then, the absolute stability of the integrated converter is solely decided by the solutions of $1 + Z_{oU}/Z_L(s) = 0$. Accordingly, the impedance ratio $Z_{oU}/Z_L(s)$ can be treated as a loop gain which determines stability of the integrated converter, as is the case with the *regular* loop gain T_{mU} of the standalone converter. In this perspective, the impedance ratio $Z_{oU}/Z_L(s)$ is referred to as the minor loop gain $T_{mn}(s)$ in the previous publication [4], [11], [13], [18]

$$T_{mn}(s) = \frac{Z_{oU}}{Z_L(s)} \tag{4}$$

The absolute stability of the integrated converter is assessed from the solutions of $1 + T_{mn}(s) = 0$. The Nyquist stability criterion will be applied to the polar plot of $T_{mn}(s)$ to judge whether the integrated converter is stable or not.

B. Polar Plot of Minor Loop Gain

The polar plot of the minor loop gain, $T_{mn}(s) = Z_{oU}/Z_L(s)$, is determined by the properties of the load impedance $Z_L(s)$ and output impedance of the standalone converter, Z_{oU}.

1) Load Impedance $Z_L(s)$: The load impedance is a cascaded connection of the filter impedance and input impedance of the regulated load converter. As demonstrated in [5], [16], [19], [20], the input impedance of a regulated converter behaves as a negative resistance, $-R_{iC}$, up to the converter's loop gain crossover frequency. Thus, the load converter is replaced with the negative resistance for the purpose of the load impedance evaluation. Figures 3(a) and 3(b) illustrate this concept. The value for the negative resistance is given by [11],

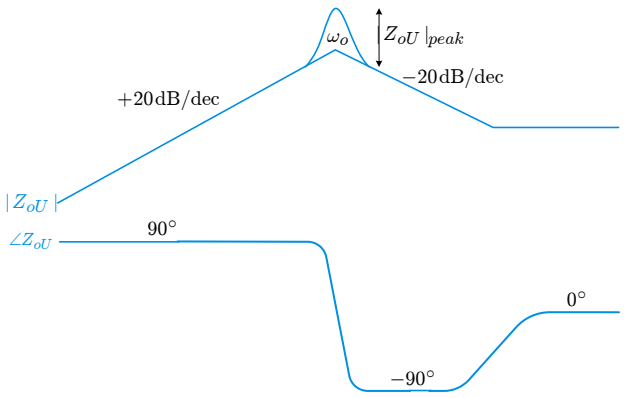


Fig. 4. Output impedance of standalone PWM dc-to-dc converter.

[19], [20]

$$-R_{iC} = -\frac{V_S}{I_S} \tag{5}$$

where V_S is the dc voltage across the input port of the load subsystem and I_S is the dc current flowing into the load subsystem. The assumption $R_{lf} \ll |R_{iC}|$ is used in (5).

From Fig. 3(b), the load impedance $Z_L(s)$ is evaluated as

$$\begin{aligned} Z_L(s) &= sL_f + R_{lf} + \left(R_{cf} + \frac{1}{sC_f}\right) \parallel (-R_{iC}) \\ &\approx -R_{iC}\frac{\left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}\right)}{1 + \frac{s}{\omega_p}} \end{aligned} \tag{6}$$

$$\text{where} \quad \omega_o = \frac{1}{\sqrt{L_f C_f}} \quad Q = \frac{1}{R_{lf} + R_{cf}}\sqrt{\frac{L_f}{C_f}}$$

$$\omega_p = -\frac{1}{C_f R_{iC}}$$

with the assumptions of $R_{iC} \gg R_{lf}$, $R_{iC} \gg R_{cf}$ and $C(R_{lf} + R_{cf}) \gg L_f/R_{iC}$. The ω_p is a right-half plane (RHP) pole, which boosts $\angle Z_L$ by 90° while bringing down $|Z_L|$ by −20 dB/dec slope. The asymptotic plots of $Z_L(s)$ are drawn in Fig. 3(c). The $|Z_L|$ follows the low-frequency asymptote of R_{iC} until it starts to decline with a −20 dB/dec slope at ω_p. At high frequencies, $|Z_L|$ increases with a 20 dB/dec slope. The $|Z_L|$ shows a resonant-type dipping around ω_o. The magnitude of dipping is given by $20\log Q$. When the filter is properly damped [3], [5], [19], [21], for example $Q < 2$, $|Z_L|$ does not show any excessive dipping. The $\angle Z_L$ starts from −180° at low frequencies, passes −135° at ω_p, and finally settles at 90° at high frequencies.

Although a simple load subsystem is used, the preceding analysis reveals the essential characteristics of common load subsystems formed with filter stages and dc-to-dc converters. The load impedance of such load subsystems largely resembles Fig. 3(c). The load impedance behaves as a negative resistance at low frequencies, exhibits a resonant-type dipping at mid-frequency band, and increases linearly at high frequencies.

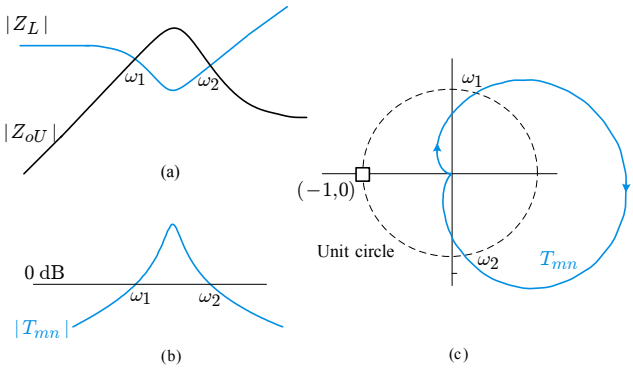


Fig. 5. Polar plot of impedance ratio Z_{oU}/Z_L as minor loop gain T_{mn}. (a) Bode plot of $|Z_{oU}|$ and Z_L. (b) Bode plot of $|T_{mn}|$. (c) Polar plot of T_{mn}.

2) Output Impedance of Standalone Converter Z_{oU}: The output impedance of the converter loaded with an ideal current sink, Z_{oU}, has been analyzed in past publications [7], [22], Figure 4 shows the asymptotic plots of typical Z_{oU} of pulsewidth modulated (PWM) converters. The Z_{oU} shows inductive characteristics at low frequencies, undergoes a resonant-type transitional peaking near the converter's loop gain crossover frequency, and finally becomes resistive at high frequencies. The magnitude of the peaking in the vicinity of the loop gain crossover frequency is determined by [14], [23]

$$|Z_{oU}|_{peak} = 20\log\frac{1}{\sqrt{2 - 2\cos \mathrm{PM}}} \tag{7}$$

where PM is the phase margin on the standalone converter. The output impedance does not produce a sharp peaking unless the phase margin is unduly small.

3) Polar Plot of minor loop gain: The polar plot of the minor loop gain is inferred from the asymptotic plots of Z_L and Z_{oU}. The typical pattern of the polar plot is depicted in Fig. 5. Figure 5(a) shows the Bode plots of $|Z_{oU}|$ and $|Z_L|$, which indicates that $|Z_{oU}|$ exceeds $|Z_L|$ in the frequency range of $\omega_1 < \omega < \omega_2$. Figure 5(b) is the Bode plot of $|T_{mn}| = |Z_{oU}|/|Z_L|$. For the frequencies $\omega_1 < \omega < \omega_2$, where $|Z_{oU}| > |Z_L|$, $|T_{mn}|$ rises above the 0 dB line. Figure 5(c) displays the polar plot of $T_{mn}(s)$. The polar plot traces a closed path, starting from and returning to the origin, as the frequency ω increases from zero to infinity. In the frequency range of $\omega_1 < \omega < \omega_2$, the polar plot travels outside the unit circle.

C. Absolute Stability

The absolute stability of the integrated converter is determined by applying the Nyquist stability criterion to the polar plot of $T_{mn}(s) = Z_{oU}/Z_L(s)$. The converter becomes unstable when the polar plot encircles the $(-1, 0)$ point. Otherwise, the converter remains stable after integration. The illustrative polar plot in Fig. 5(c) is a stable case.

Figure 6 is the illustrative plots for $|Z_{oU}|$ and $|Z_L|$, along with the polar plot of $T_{mn}(s) = Z_{oU}/Z_L(s)$. Three different load impedances, $Z_{L1}(s)$, $Z_{L2}(s)$, and $Z_{L3}(s)$, are considered. The $|Z_{oU}|$ and $|Z_L|$ overlap at the frequencies where $|Z_L|$ dips into the valley value while $|Z_{oU}|$ attains its peak value. The previous analysis indicates that the phase of Z_{oU} varies between 90° >

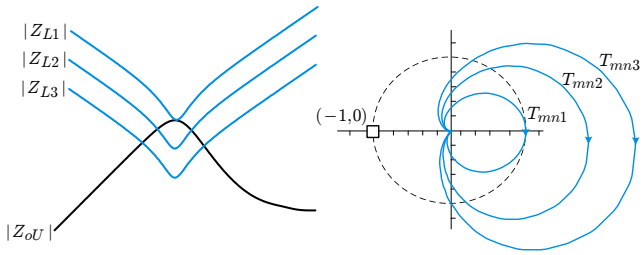


Fig. 6. Bode plot and polar plot of minor loop gain.

$\angle Z_{oU} > -90°$ over the impedance overlap, while the phase of $Z_L(s)$ varies between $-90° < \angle Z_L < 90°$. Thus, the phase of $T_{mn}(s)$, $\angle T_{mn} = \angle Z_{oU} - \angle Z_L$, alters between

$$\begin{aligned} 90° - (-90°) \; &> \angle T_{mn} > \; -90° - (90°) \\ \Rightarrow \quad 180° \; &> \angle T_{mn} > \; -180° \end{aligned}$$

As the overlap grows larger, the polar plot travels closer to the $(-1, 0)$ point. However, the polar plot does not encircle the $(-1, 0)$ point because $\angle T_{mn}$ is bounded between $180° > \angle T_{mn} > -180°$. This indicates that the integration does not lead to instability.

The above argument is generalized in Fig. 7, which illustrates the impedance overlaps and polar plots of $T_{mn}(s)$ for four different cases. A typical Bode plot of Z_{oU} is shown in Fig. 7. The phase of Z_{oU} starts from $90°$ at low frequencies, drops to $-90°$ over the mid-frequency peaking, and settles to $0°$ at high frequencies. On the other hand, the phase of the load impedance alters between $-90° < \angle Z_L < 90°$ over the impedance overlap. To predict the evolution of the polar plot, the boundaries of $\angle T_{mn} = \angle Z_{oU} - \angle Z_L$ are evaluated for the four different cases.

- **Case A:** $90° - (-90°) > \angle\left(Z_{oU}/Z_L\right) > 90° - (90°)$
  $\Rightarrow \quad 180° > \angle\left(Z_{oU}/Z_L\right) > 0°$
- **Case B:** $90° - (-90°) > \angle\left(Z_{oU}/Z_L\right) > -90° - (90°)$
  $\Rightarrow \quad 180° > \angle\left(Z_{oU}/Z_L\right) > -180°$
- **Case C:** $-90° - (-90°) > \angle\left(Z_{oU}/Z_L\right) > -90° - (90°)$
  $\Rightarrow \quad 0° > \angle\left(Z_{oU}/Z_L\right) > -180°$
- **Case D:** $0° - (-90°) > \angle\left(Z_{oU}/Z_L\right) > 0° - (90°)$
  $\Rightarrow \quad 90° > \angle\left(Z_{oU}/Z_L\right) > -90°$

The patterns of the polar plots are shown in Fig. 7. The polar plots do not encircle the $(-1, 0)$ point for all the four cases and the integrated converter always remains stable.

For some cases, $|Z_L|$ is larger than $|Z_{oU}|$ for all frequencies, thereby initially precluding the possibility of any impedance overlap. The integrated converter is invariably stable for this case. Actually, avoiding the overlap is the sufficient condition for stability. However, this requirement is overly conservative and restrictive. The impedance overlap usually occurs after integration. However, for most practical cases, the overlap happens in the similar manner to those of Fig. 7. Therefore, the converter continues to be stable despite the presence of the impedance overlap after integration, provided that the standalone converter secures a reasonable phase margin and the filter stage is adequately damped [3], [19].

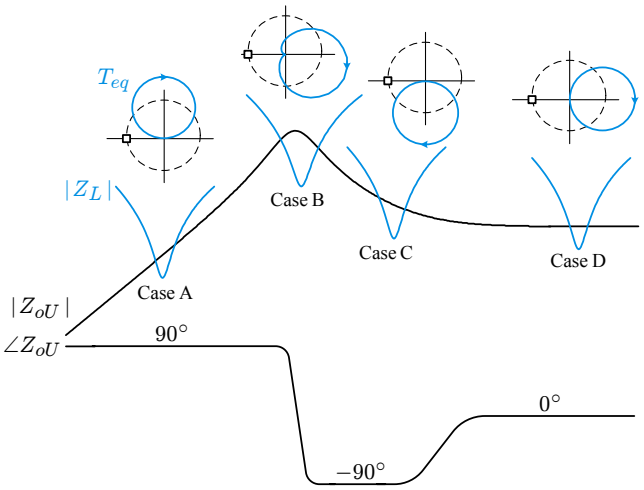


Fig. 7. Impedance overlaps and polar plots of Z_{oU}/Z_L for general cases.

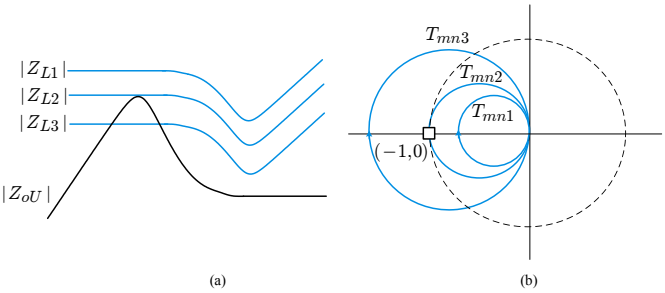


Fig. 8. Hypothetical example of instability. (a) Bode plot of $|Z_{oU}|$ and $|Z_L|$. (b) Polar plot of Z_{oU}/Z_L.

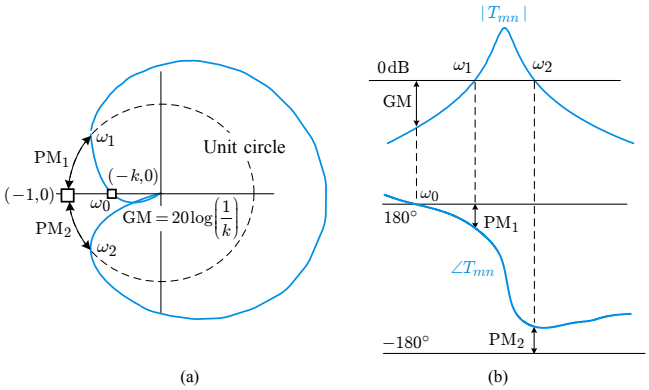
Yet, the risk of instability still exists when a poorly-designed converter is integrated with an ill-conditioned load subsystem. A hypothetical example is shown in Fig. 8, where a dc-to-dc converter is integrated with certain load impedances. In this example, the impedance overlap happens at the low frequencies where the load impedance behaves as a negative resistance, $-R_{iC}$. The phase of the load impedance is now fixed at $\angle Z_L = -180°$ and the phase of $T_{mn}(s)$ thus changes between

$$\begin{aligned} 90° - (-180°) > \angle T_{mn} > -90° - (-180°) \\ \Rightarrow \quad 270° > \angle T_{mn} > 90° \end{aligned}$$

The polar plot passes the $(-1, 0)$ point when $|Z_L|$ and $|Z_{oU}|$ touch each other, and encircles the $(-1, 0)$ point when the two impedances overlap. These cases break the Nyquist stability criterion and lead to instability. The two roots of $1 + Z_{oU}/Z_L(s) = 0$ lie on the imaginary axis when the polar plot passes $(-1, 0)$ point, and penetrates into the RHP of s-plane when the polar plot encircles the $(-1, 0)$ point.

The unstable example in Fig. 8 is conceived based on the following assumptions.

1) The output impedance of the standalone converter produces a peaking at very low frequencies. This would happen only provided that the voltage feedback is improperly designed so that the loop gain crossover occurs at unusually low frequencies. When the standard design procedures [14],



(a) (b)

Fig. 9. Phase margin and gain margin of minor loop gain. (a) Polar plot representation. (b) Bode plot representation.

[15] are followed, the output impedance of a standalone converter does not generate such a low-frequency peaking.

2) The parameters of the filter stage are unusually selected so that the load impedance exhibits a dipping at higher frequencies than normal cases. The resulting filter stage would not provide sufficient filtering and EMI standards won't be met [3].

The previous arguments insinuate that instability shown in Fig. 8 will not take place in practical applications.

D. Stability Margins of Minor Loop Gain

The concept of the stability margins is extended to the minor loop gain, $T_{mn}(s) = Z_{oU}/Z_L(s)$, to define its phase margin and gain margin. As will be demonstrated later, the stability margins of the minor loop gain play an important role in assessing the relative stability of the integrated converter. Figure 9 illustrates the phase margin and gain margin, defined on both the polar plot and Bode plot of the minor loop gain $T_{mn}(s)$.

Phase Margin: Two different phase margins are defined at ω_1 and ω_2, where the polar plot crosses the unit circle, or equivalently $|T_{mn}|$ passes the 0 dB line

- Phase margin at ω_1: $\mathrm{PM}_1 = 180° - \angle T_{mn}(j\omega_1)$
- Phase margin at ω_2: $\mathrm{PM}_2 = \angle T_{mn}(j\omega_2) - (-180°)$

Figure 9(a) depicts the phase margins on the polar plot, while Fig. 9(b) portraits the phase margins on the Bode plot.

Gain Margin: The gain margin is defined at the frequency ω_0, where the polar plot crosses the $-$ real axis, or equivalently $\angle T_{mn}$ falls to 180°. When the polar plot crosses the $(-k, 0)$ point, the gain margin is given by $\mathrm{GM} = 20\log(1/k)$. The gain margin is illustrated in Fig. 9(a) and Fig. 9(b).

The phase and gain margins specify the additional phase change and magnitude increase that can be added to $T_{mn}(s) = Z_{oU}/Z_L(s)$ before the converter encounters instability. More importantly, the stability margins serve as barometers for the closed-loop performance of the converter. A small phase margin is an indication of a peaking in transfer functions and oscillatory behavior in transient responses [14], [23]. Most importantly, the stability margins of the minor loop gain often become the stability margins of the loop gain of the integrated converter. For example, the phase margin PM_1, defined for the minor loop gain in Fig. 9, frequently becomes the phase margin of the integrated converter, as will be shown in the next section.

III. Converter Loop Gain and Relative Stability

Although the absolute stability is determined by the minor loop gain, the relative stability should be assessed from the loop gain of the converter integrated with the load subsystem. The load subsystem seldom destabilizes a previously stable upstream converter. However, the load impedance usually induces significant changes in the converter dynamics, yielding very complex loop gain characteristics. This section investigates the loop gain of the integrated converter and examines the impact of the load subsystem on the relative stability of the converter.

A. Converter Loop Gain Analysis

The loop gain expression of the integrated converter, $T_{mL}(s)$ given in (1), is written as

$$T_{mL}(s) = \frac{T_{mU}}{1 + T_{mn}(s) + T_{mU}T_{mn}(s)} \tag{8}$$

where T_{mU} is the loop gain of the standalone converter and $T_{mn}(s) = Z_{oU}/Z_L(s)$ is the minor loop gain. The converter loop gain will remain unaffected, $T_{mL}(s) \approx T_{mU}$, when the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$ are simultaneously met for all frequencies. However, this requirement is usually not satisfied and the loop gain characteristics are thus to be altered by $Z_L(s)$. The expression (8) is used to characterize and construct the converter loop gain using Bode plot technique.

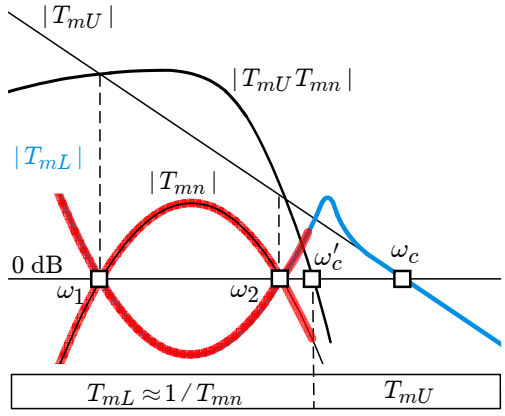
Figure 10 shows the construction of $|T_{mL}|$ based on (8). The following assumptions are made to simplify the $|T_{mL}|$ construction without loss of generality.

1) The loop gain of the standalone converter, T_{mU}, has an integrator structure and crosses the 0 dB line at ω_c with a phase margin of PM_c.

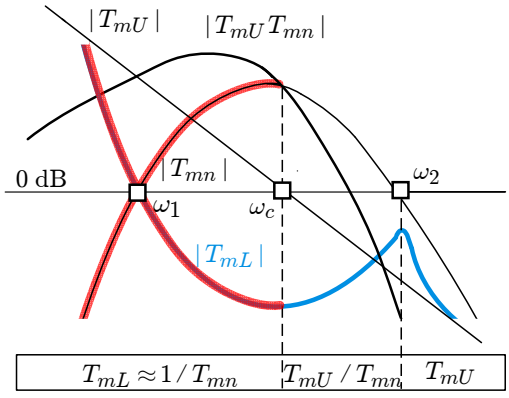
2) The minor loop gain, $|T_{mn}| = |Z_{oU}/Z_L|$, crosses the 0 dB line at ω_1 and ω_2 with the respective phase margin of PM_1 and PM_2.

In Fig. 10, the asymptotic plot for $|T_{mU}\,T_{mn}|$ is drawn by adding $|T_{mU}|$ and $|T_{mn}|$. As shown in Fig. 10, the construction of $|T_{mL}|$ is classified into the three cases, based on the locations of the crossover frequencies of $|T_{mn}|$ and $|T_{mU}|$.

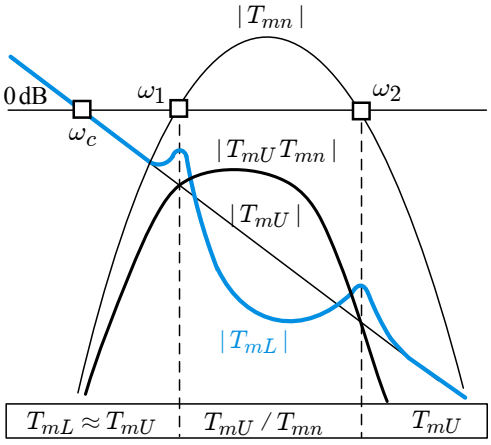
Case A: Shown in Fig. 10(a) is Case A, where the crossover frequencies of $|T_{mn}|$ come earlier than the crossover frequency of $|T_{mU}|$, $\omega_1 < \omega_2 < \omega_c$. Up to the frequency where $|T_{mU}\,T_{mn}|$ crosses the 0 dB line, denoted as ω_c' in Fig. 10(a), the conditions $1 \ll |T_{mU}\,T_{mn}|$ and $|T_{mn}| \ll |T_{mU}\,T_{mn}|$ prevail. For the frequencies



(a)



(b)



(c)

Fig. 10. Construction of loop gain of integrated converter. (a) Case A: $\omega_1 < \omega_2 < \omega_c$. (b) Case B: $\omega_1 < \omega_c < \omega_2$. (c) Case C: $\omega_c < \omega_1 < \omega_2$.

below ω_c', the loop gain is thus given by

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mU}}{1+T_{mn}(s)+T_{mU}T_{mn}(s)} \\ &\approx \frac{T_{mU}}{T_{mn}(s)+T_{mU}T_{mn}(s)} \\ &\approx \frac{T_{mU}}{T_{mU}T_{mn}(s)} = \frac{1}{T_{mn}(s)} \end{aligned}$$

Thus, $|T_{mL}|$ follows the mirror image of $|T_{mn}|$ reflected on the 0 dB axis, as highlighted with the red curve in Fig. 10(a). For the frequencies beyond ω_c' where the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$ are met, the loop gain of the integrated converter trails the loop gain of the standalone converter, $T_{mL}(s) \approx T_{mU}$. A peaking may occur at ω_c' where $|T_{mL}|$ diverts from $1/|T_{mn}|$ to $|T_{mU}|$, as shown in Fig. 10(a).

The $|T_{mL}|$ exhibits very involved characteristics, even crossing the 0 dB line three times. However, the converter remains stable as far as the minor loop gain $T_{mn}(s)$ meets the Nyquist stability criterion. With multiple 0 dB crossovers, the phase margin is not uniquely determined for this case.

Case B: Figure 10(b) shows Case B, where the crossover frequency of $|T_{mU}|$ appears between the crossover frequencies of $|T_{mn}|$, $\omega_1 < \omega_c < \omega_2$. For the frequencies below ω_c where the conditions $1 \ll |T_{mU}\,T_{mn}|$ and $|T_{mn}| \ll |T_{mU}\,T_{mn}|$ hold, $|T_{mL}|$ follows $1/|T_{mn}|$. On the other hand, the conditions $1 \ll |T_{mn}|$ and $|T_{mU}\,T_{mn}| \ll |T_{mn}|$ are valid in the frequency range of $\omega_c < \omega < \omega_2$. These conditions simplify loop gain expression to

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mU}}{1+T_{mn}(s)+T_{mU}T_{mn}(s)} \\ &\approx \frac{T_{mU}}{T_{mn}(s)+T_{mU}T_{mn}(s)} \approx \frac{T_{mU}}{T_{mn}(s)} \end{aligned}$$

thus indicating the loop gain magnitude is formed by the relationship of $|T_{mL}| = |T_{mU}| - |T_{mn}|$. At the frequencies after ω_2, $|T_{mL}|$ tracks $|T_{mU}|$ with the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$. A peaking could appear at the second crossover frequency of $|T_{mn}|$, ω_2. The magnitude of the peaking is inversely proportional to the phase margin of $|T_{mn}|$ at ω_2, PM_2 [14].

For Case B, the $|T_{mL}|$ crossover occurs at ω_1, the first crossover frequency of $|T_{mn}|$. The phase margin of $T_{mL}(s)$ is the same as the phase margin of $T_{mn}(s)$ for the following reason.

1) The phase margin of $T_{mL}(s)$ is determined by the s-domain locations of the solutions of the equation $1 + T_{mL}(s) = 0$. Likewise, the phase margin of $T_{mn}(s)$ is decided by the locations of the roots of $1 + T_{mn}(s) = 0$.
2) With the knowledge of $T_{mL}(s) = 1/T_{mn}(s)$, the equation $1 + T_{mL}(s) = 0$ is rewritten as

$$1+T_{mL}(s) = 0 \;\Rightarrow\; 1+1/T_{mn}(s) = 0 \;\Rightarrow\; 1+T_{mn}(s) = 0$$

3) Thus, $T_{mL}(s)$ and $T_{mn}(s)$ have the same phase margin.

Case C: Figure 10(c) displays Case C with $\omega_c < \omega_1 < \omega_2$. The $|T_{mL}|$ largely trails $|T_{mU}|$, except for the frequency range of $\omega_1 < \omega < \omega_2$, where $|T_{mL}|$ tracks $|T_{mU}/T_{mn}|$ due to the conditions $1 \ll |T_{mn}|$ and $|T_{mU}T_{mn}| \ll |T_{mn}|$. The crossover frequency and phase margin of the integrated converter are the same as those of the standalone converter. The load impedance does not alter the crossover frequency and phase margin of the loop gain, because the load impedance becomes effective after the crossover frequency of T_{mU}.

The outcomes of the preceding loop gain analysis are summed up in Table I. Among the three cases, Case B will occur most frequently in practical applications.

TABLE I. SUMMARY OF LOOP GAIN ANALYSIS

	T_{mL} from low to mid frequencies	0 dB crossover frequency of T_{mL}	Phase margin of T_{mL}
Case A: $\omega_1 < \omega_2 < \omega_c$	$T_{mL} \approx 1/T_{mn}$	ω_1, ω_2, and ω_c	Not uniquely determined
Case B: $\omega_1 < \omega_c < \omega_2$	$T_{mL} \approx 1/T_{mn}$	ω_1	PM_1
Case C: $\omega_c < \omega_1 < \omega_2$	$T_{mL} \approx T_{mU}$	ω_c	PM_c

The peaking in $|Z_{oU}|$ usually appears at the crossover frequency of $|T_{mU}|$. On the other hand, the impedance overlap between $|Z_{oU}|$ and $|Z_L|$ typically takes place at the frequencies where $|Z_{oU}|$ reaches its peak. Therefore, the crossover frequency of $|T_{mU}|$ lies inside the frequency range of the impedance overlap — Case B in Fig. 10.

For Case B, the crossover frequency and phase margin of $T_{mL}(s)$ are determined by those of the minor loop gain $T_{mn}(s)$. Therefore, although the loop gain is altered substantially over a wide frequency range, the converter remains stable as far as $T_{mn}(s)$ meets the Nyquist stability criterion. Furthermore, for the frequencies before T_{mu} crossover frequency, the loop gain is given by the mirror image of the minor loop gain reflected by the 0 dB axis. Thus, the converter retains good transient responses provided that the phase margin and the crossover frequency of $T_{mn}(s)$ are not unduly small and narrow.

B. Experimental Results

For the experimental verification of the preceding discussions, an illustrative example is given in Fig. 11 for Case B. Figure 11 shows a two-stage dc-to-dc power conversion system, where a current-mode controlled boost converter is integrated with a regulated buck converter through a filter stage. Both the boost converter and buck converter are designed based on standard design procedures [14], [15].

The two-stage power conversion system shown in Fig. 11 was built and the loop gain and step load response of the boost converter were measured with the load subsystem. The same experiment was performed after replacing the load subsystem with a current sink load. Figure 12(a) shows the measured loop gains of the integrated boost converter, $T_{mL}(s)$, and standalone boost converter, T_{mU}, in comparison with the small-signal simulation results. Close correlations between the experimental measurements and analytical predictions support the validity and accuracy of the analyses.

Figure 12(b) exhibits the transient responses of the integrated and standalone boost converters. The upper traces show the output voltage, $v_O(t)$, and inductor current, $i_L(t)$, of the boost converter connected with a current sink load in response to 2 A $\rightarrow$ 1.5 A $\rightarrow$ 2 A changes in the sink current. The lower traces are the waveforms of the boost converter connected with the load subsystem of Case B, where 92 W $\rightarrow$ 69 W $\rightarrow$ 92 W power changes are introduced to the buck converter downstream. The load subsystem makes the transient response somewhat

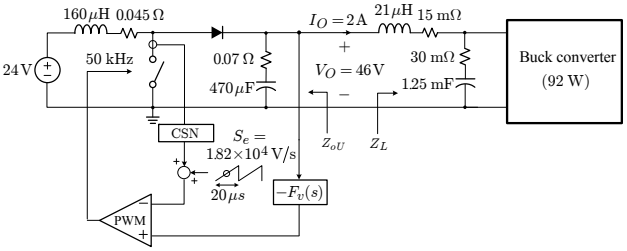


Fig. 11. Two-stage power conversion system consisting of current-mode controlled boost converter, filter stage, and regulated buck converter. The CSN is the current sensing network with the dc gain $R_i = 0.45$, PWM is the pulsewidth modulation block, and $F_v(s) = 3.69 \times 10^3(1 + s/2\pi \cdot 262)/(s(1 + s/2\pi \cdot 5.68 \times 10^3))$ is the voltage feedback compensation.

oscillatory and sluggish. Nonetheless, the converter retains stability and performance after integration. Finally, Fig. 12(c) illustrates the minor loop gain for the load subsystem of Case B. As predicted, the crossover frequency and phase margin of the minor loop gain are the same as those of the loop gain of the boost converter integrated with the load subsystem of Case B.

IV. CONCLUSIONS

This paper investigated stability of dc-to-dc converters deriving another converter downstream through a filter stage. The paper demonstrated that the input impedance of the downstream filter/converter stage, namely the load impedance, dictates both the absolute and relative stabilities of the upstream converter. All the information about stability can be extracted from the minor loop gain, defined as the ratio of the output impedance of the standalone converter to the load impedance.

The load impedance does not alter the existing poles of the standalone converter, but creates new poles which determines the absolute stability of the integrated converter. The integrated converter becomes unstable only if the minor loop gain violates the Nyquist stability criterion. However, this instability seldom occurs provided that the upstream converter, filter stage, and load converter are built based on the standard design procedures.

The load impedance invariably affects the loop gain characteristics of the upstream converter. The influence of the load impedance can be substantial in magnitude and wide in frequency range. The integrated converter could exhibit very involved loop gain characteristics, even crossing the 0 dB line three times. Nonetheless, the integrated converter always remains stable as far as the minor loop gain meets the Nyquist stability criterion.

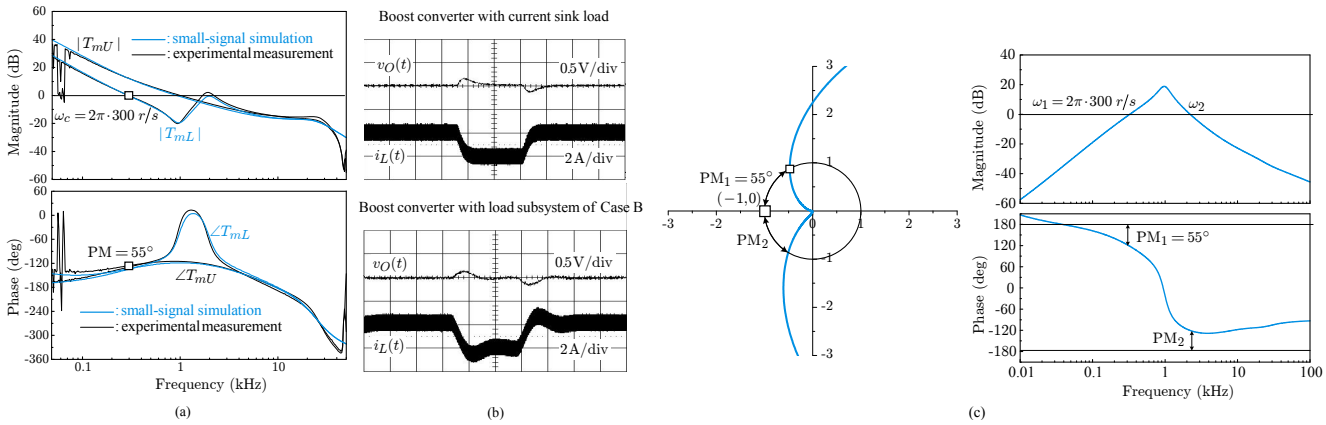


Fig. 12. Experimental verification of boost converter performance for Case B. (a) Loop gain. (b) Step load response. (c) Minor loop gain.

The relative stability is determined by the loop gain of the integrated converter. The graphical Bode plot analysis was employed to yield a simple method to predict the asymptotic plot, crossover frequency, and phase margin of the loop gain of the integrated converter. The outcomes of this analyses are summarized in Fig. 10 and Table I. Very interestingly, the loop gain of the integrated converter is largely and frequently given by the mirror image of the minor loop gain reflected by the 0 dB axis. for the frequency range of practical importance. For this case, the crossover frequency and phase margin of the integrated converter are identical to those of the minor loop gain. When the minor loop gain has a sufficient phase margin and high crossover frequency, the integrated converter exhibits stability and good transient responses. Thus, all the criteria for the stability and performance of the integrated converter can be predicted and enhanced by investigating and improving the minor loop gain.

REFERENCES

[1] B. Choi, B. Cho, and S.-S. Hong, "Dynamics and control of dc-to-dc converters driving other converters downstream," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 46, no. 10, pp. 1240–1248, Oct 1999.

[2] W. Tabisz, M. Jovanovic, and F. Lee, "Present and future of distributed power systems," in *Applied Power Electronics Conference and Exposition, APEC '92. Conference Proceedings 1992., Seventh Annual*, Feb 1992, pp. 11–18.

[3] B. Choi and B. Cho, "Intermediate line filter design to meet both impedance compatibility and EMI specifications," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 583–588, Sep 1995.

[4] X. Zhang, X. Ruan, and C. Tse, "Impedance-based local stability criterion for DC distributed power systems," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 62, no. 3, pp. 916–925, March 2015.

[5] M. Wu and D. Lu, "A novel stabilization method of LC input filter with constant power loads without load performance compromise in DC Microgrids," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1–1, 2014.

[6] T. Suntio, M. Hankaniemi, and M. Karppanen, "Analysing the dynamics of regulated converters," *Electric Power Applications, IEE Proceedings* -, vol. 153, no. 6, pp. 905–910, November 2006.

[7] B. Choi, J. Kim, B. Cho, S. Choi, and C. Wildrick, "Designing control loop for DC-to-DC converters loaded with unknown AC dynamics," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 925–932, Aug 2002.

[8] M. Karppanen, T. Suntio, and M. Sippola, "Dynamical characterization of input-voltage-feedforward-controlled buck converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1005–1013, April 2007.

[9] P. Li and B. Lehman, "Performance prediction of DC-DC converters with impedances as loads," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 201–209, Jan 2004.

[10] D. Lee, B. Choi, J. Sun, and B. Cho, "Interpretation and prediction of loop gain characteristics for switching power converters loaded with general load subsystem," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, June 2005, pp. 1024–1029.

[11] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *IEEE Industry Applications Society Annual Meeting*, October 1976, pp. 366 –382.

[12] B. Choi, D. Kim, D. Lee, S. Choi, and J. Sun, "Analysis of input filter interactions in switching power converters," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 452–460, March 2007.

[13] F. Liu, J. Liu, H. Zhang, and D. Xue, "Stability issues of $Z+Z$ type cascade system in hybrid energy storage system (HESS)," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5846–5859, Nov 2014.

[14] B. Choi, *Pulsewidth Modulated DC-to-DC Power Conversion: Circuits, Dynamics, and Control Designs*. John Wiley & Sons, 2013.

[15] R. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 36–52, Jan 1989.

[16] M. Hankaniemi, M. Karppanen, and T. Suntio, "Load-imposed instability and performance degradation in a regulated converter," *Electric Power Applications, IEE Proceedings* -, vol. 153, no. 6, pp. 781–786, November 2006.

[17] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2001.

[18] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for DC power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3525–3535, Sept 2014.

[19] M. Cespedes, L. Xing, and J. Sun, "Constant-power load system stabilization by passive damping," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1832–1836, July 2011.

[20] Y. Li, K. Vannorsdel, A. Zirger, M. Norris, and D. Maksimovic, "Current mode control for boost converters with constant power loads," *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 59, no. 1, pp. 198–206, Jan 2012.

[21] X. Zhang, X. Ruan, H. Kim, and C. K. Tse, "Adaptive active capacitor converter for improving stability of cascaded DC power supply system," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1807–1816, April 2013.

[22] S. Abe, M. Hirokawa, M. Shoyama, and T. Ninomiya, "Optimal intermediate bus capacitance for system stability on distributed power architecture," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, June 2008, pp. 611–616.

[23] S. Vesti, T. Suntio, J. Oliver, R. Prieto, and J. Cobos, "Impedance-based stability and transient-performance assessment applying maximum peak criteria," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2099–2104, May 2013.