CHAPTER 1

LOAD-COUPLED CONVERTERS AND LOADING EFFECTS

In the last chapter, we studied the design and analysis method for converters intended for general dc power conversion applications. A converter powered from an ideal voltage source and loaded with a current sink was defined as an *uncoupled converter*. The uncoupled converter allows us to conceptually separate an individual converter from the system. This permits us to execute the control design without any prior knowledge about the source and load subsystems. Later, we revealed that uncoupled converters can be designed using the conventional design procedures, originally intended for the resistive case.

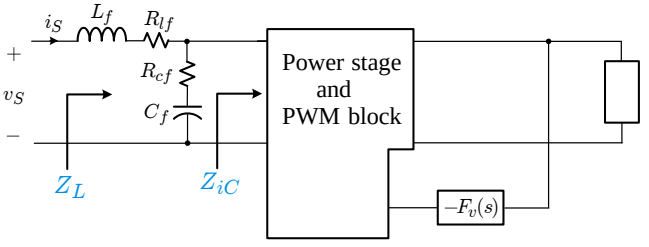


Figure 1.1 Load subsystem as combination of filter stage and converter.

We employed Middlebrook's extra element theorem (EET) to develop general analysis methodologies for the converters coupled with a non-ideal source or practical load. Considering the source and load impedances as the extra elements, we applied the EET to express the performance of the coupled converters as combinations of the transfer functions of the uncoupled converter and impedances of the extra elements. The outcomes of this analysis are summarized in Tables **??** and **??**. We now step through the detailed dynamic analysis of the coupled converters.

The converter coupled with a general load subsystem, yet still powered from an ideal voltage source, was denoted as the *load-coupled converter*. Load-coupled converters usually encounter certain changes in their performance. Influences of the load subsystem are called the *loading effects*. Illuminations of the loading effects were given in Example **??** in the previous chapter. The current section investigates the origins, dynamics, and consequences of the loading effects.

We first study the input impedance of load subsystems, which is referred to as the load impedance. Then, we examine the impacts of the load impedance, or the loading effects, on stability and other performance of load-coupled converters. In particular, the impacts of the load impedance on the loop gain and input impedance of the upstream converter are analyzed in detail. This chapter provides the sufficient knowledge to predict and comprehend the converter performance under the strong loading effects.

1.1 LOAD SUBSYSTEM AND LOAD IMPEDANCE

The load subsystem is commonly identified as a combination of filter stages and other converters. Figure 1.1 shows a simple load subsystem, configured with a single-stage filter and a closed-loop controlled converter. This load subsystem will couple with a converter upstream and affect the dynamics of the load-coupled converter. As the prerequisite for the study of load-coupled converters, we first evaluate the input impedance of the load subsystem, namely the load impedance $Z_L(s)$.

The load impedance $Z_L(s)$ is a complex quantity due to the presence of the converter stage. An exact evaluation of $Z_L(s)$ through conventional circuit analyses soon becomes intractable. Here, we use the EET and graphical method to make the analysis manageable and practical. Although the analysis procedures are lengthy,

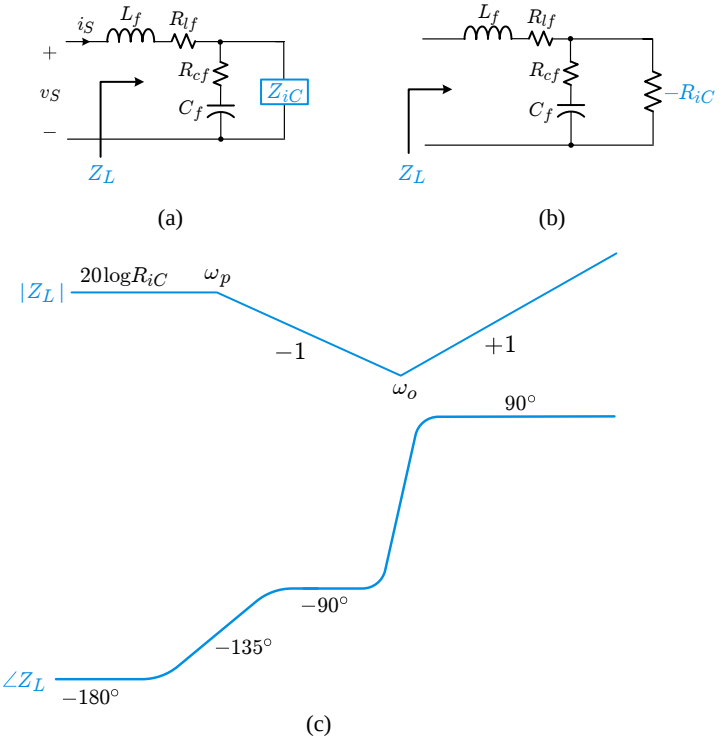


Figure 1.2 Load impedance evaluation. (a) Load subsystem. (b) Circuit model. (c) Asymptotic plots for Z_L.

the results are rather simple. We first present the final results and later discuss the analytical details.

1.1.1 Results of Load Impedance Analysis

The load impedance $Z_L(s)$ is a cascaded connection of the filter impedance and the input impedance of the regulated converter, $Z_{iC}(s)$ in Fig. 1.1. The converter input impedance of a regulated converter, $Z_{iC}(s)$, behaves as a negative resistance up to the converter's loop gain crossover frequency. Thus, the regulated converter is replaced with a single negative resistance for the load impedance evaluation. Figures 1.2(a) and 1.2(b) illustrate this concept. The input impedance of the regulated converter, $Z_{iC}(s)$ in Fig. 1.2(a), is replaced with the negative resistance, $-R_{iC}$ in Fig. 1.2(b).

The value of the negative resistance is given by [†]

$$\boxed{-R_{iC} = -\frac{V_S}{I_S}} \tag{1.1}$$

where V_S is the dc voltage across the input port of the load subsystem and I_S is the dc current flowing into the load subsystem. The negative resistance $-R_{iC}$ is an approximation of the input impedance of the regulated converter. The validity of this approximation will be shown later. From Fig. 1.2(b), the load impedance $Z_L(s)$ is evaluated as

$$\begin{aligned} Z_L(s) &= sL_f + R_{lf} + \left(R_{cf} + \frac{1}{sC_f}\right) \parallel (-R_{iC}) \\ &= \boxed{-R_{iC}\frac{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}}{1 + \dfrac{s}{\omega_p}}} \end{aligned} \tag{1.2}$$

where

$$\omega_o = \sqrt{\frac{R_{lf} - R_{iC}}{R_{cf} - R_{iC}}\frac{1}{L_f C_f}} \approx \frac{1}{\sqrt{L_f C_f}} \tag{1.3}$$

$$Q = \frac{1}{\omega_o}\frac{R_{lf} - R_{iC}}{L_f + C_f\big(R_{lf}R_{cf} - R_{iC}(R_{lf} + R_{cf})\big)} \approx \frac{1}{R_{lf} + R_{cf}}\sqrt{\frac{L_f}{C_f}} \tag{1.4}$$

$$\omega_p = \frac{1}{C_f(R_{cf} - R_{iC})} \approx -\frac{1}{C_f R_{iC}} \tag{1.5}$$

with the assumptions of $R_{iC} \gg R_{cf}$, $R_{iC} \gg R_{lf}$, and $C_f(R_{lf} + R_{cf}) \gg L_f/R_{iC}$. The ω_p in (1.5) is a right-half plane (RHP) pole [‡], which boosts $\angle Z_L$ by 90° while bringing down $|Z_L|$ by -20 dB/dec slope. The asymptotic plots of $Z_L(s)$ are drawn in Fig. 1.2(c). The $|Z_L|$ follows the low-frequency asymptote of R_{iC} before rolling down with a -20 dB/dec slope at ω_p. At high frequencies, $|Z_L|$ increases with a 20 dB/dec slope. The $\angle Z_L$ starts from -180° at low frequencies, passes -135° at ω_p, and finally settles at 90° at high frequencies.

Although a simple load subsystem is used, the preceding analysis reveals the common characteristics of general load subsystems, consisting of filter stages and converters. The load impedance behaves as a negative resistance at low frequencies,

[†] It can be shown that the expression (1.1) is equivalent to the previous equation of (**??**), under assumption that the converter operates without power loss.

[‡] The RHP pole in $Z_L(s)$ does not indicate that the load subsystem is unstable. For stability assessment, the input admittance $Y_L(s)$ should be considered rather than the input impedance $Z_L(s)$, because $Y_L(s) = \hat{\imath}_s(s)/\hat{v}_s(s)$ is the transfer function that relates the input variable of the load subsystem, $\hat{v}_s(s)$, to the output variable, $\hat{\imath}_s(s)$. The RHP pole in $Z_L(s)$ becomes an RHP zero in $Y_L(s)$.

exhibits a transitional dipping at mid-frequency band, and increases linearly at high frequencies.

The next two sections present the detailed load impedance analysis to provide the theoretical background for Fig. 1.2. The first section deals with the asymptotic analysis of the load impedance using the EET. The ensuing section discusses the validity of replacing the converter with a negative resistance.

1.1.2 Load Impedance Analysis Using EET

The load impedance is analyzed using the extra element theorem (EET). Figure 1.3 illustrates the application of the EET. The $Z_{iC}(s)$ in Fig. 1.3 denotes the input impedance of the converter. By designating $Z_{iC}(s)$ as an extra element, Fig. 1.3(a) is modified to Fig. 1.3(b) and subsequently redrawn into Fig. 1.3(c) for the EET application. The load impedance $Z_L(s)$ is expressed as

$$Z_L(s) = \frac{\hat{v}_s(s)}{\hat{i}_s(s)}_{Z_{iC}\neq\infty} = Z_{if\infty}\frac{1+\dfrac{\bar{\zeta}_{iC}(s)}{Z_{iC}(s)}}{1+\dfrac{\bar{z}_{iC}(s)}{Z_{iC}(s)}} \tag{1.6}$$

by applying the EET to Fig. 1.3. The open-circuit transfer gain $Z_{if\infty}$ is the input impedance of the filter stage evaluated with the converter removed: $Z_{iC}(s) = \infty$. The null driving point impedance, $\bar{\zeta}_{iC}(s) = v_T(s)/i_T(s)_{\hat{v}_s=0}$, is the output impedance of the filter stage assessed with the input port shorted. The null driving point impedance is denoted as the short-circuit filter output impedance, Z_{of0}.

The driving point impedance, $\bar{z}_{iC}(s) = v_T(s)/i_T(s)_{\hat{i}_s=0}$, is the filter output impedance determined with the input port opened, referred to as the open-circuit filter output impedance, $Z_{of\infty}$. The circuit illustrations of $Z_{if\infty}$, $Z_{of\,0}$, and $Z_{of\infty}$ are given in Fig. 1.4.

The load impedance $Z_L(s)$ is now expressed as

$$Z_L(s) = Z_{if\infty}\frac{1+\dfrac{Z_{of0}}{Z_{iC}(s)}}{1+\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \tag{1.7}$$

The graphical analysis method will be applied to (1.7) to portray the asymptotic behavior of the load impedance. For this purpose, it is necessary to examine the frequency responses of the four impedances, $Z_{iC}(s)$, $Z_{if\infty}$, Z_{of0}, and $Z_{of\infty}$ in (1.7).

The input impedance of the regulated converter, $Z_{iC}(s)$, will be analyzed in a later section. Based on the results of the upcoming analysis, the general shape of $|Z_{iC}|$ is depicted in Fig. 1.5(a). The $Z_{iC}(s)$ behaves as a negative resistance at low frequencies. This low-frequency asymptote stretches beyond mid frequencies. The

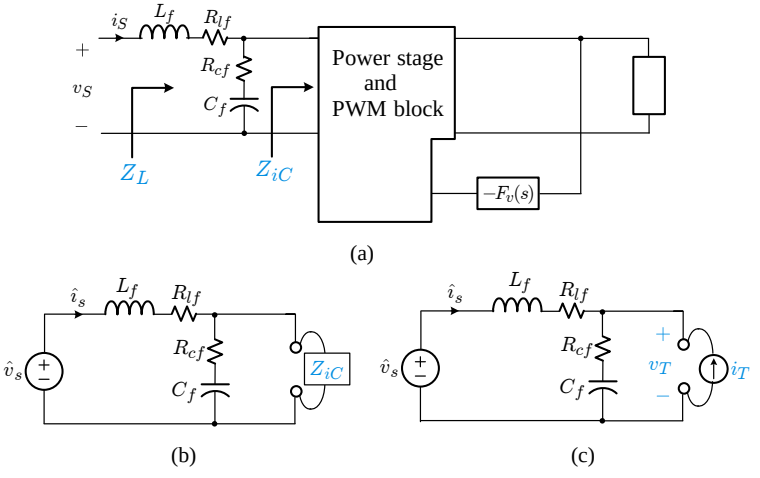


Figure 1.3 Load subsystem representations. (a) Load subsystem. (b) Representation of load subsystem using converter input impedance, Z_{iC}. (c) Modification of (b) for EET application.

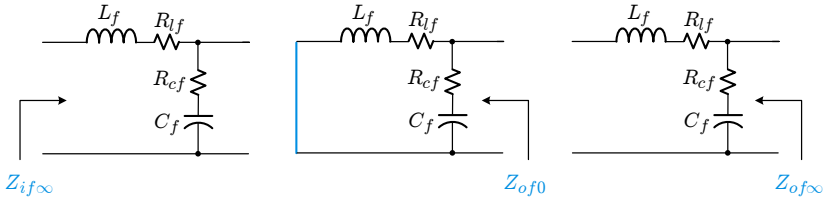


Figure 1.4 Illustrations of $Z_{if\infty}$, Z_{of0}, and $Z_{of\,\infty}$.

$|Z_{iC}|$ often undergoes a transitional dipping near the loop gain crossover frequency of the converter, marked as ω_c in Fig. 1.5(a), and rises linearly thereafter.

The asymptotic plots for $Z_{if\infty}$, Z_{of0}, and $Z_{of\infty}$ can easily be drawn using the Bode plot technique. Figure 1.5(b) shows the asymptotic plots of $|Z_{if\infty}|$, $|Z_{of0}|$, and $|Z_{of\infty}|$ together with $|Z_{iC}|$. As shown in Fig. 1.5(b), the condition $|Z_{of0}| \ll |Z_{iC}|$ is met for all frequencies when the filter is properly designed. Justifications for this statement will be given in a later chapter which deals with analysis and design of filter stages. From the $Z_L(s)$ expression in (1.7) and Fig. 1.5(b), the load impedance $Z_L(s)$ can be approximated as follows.

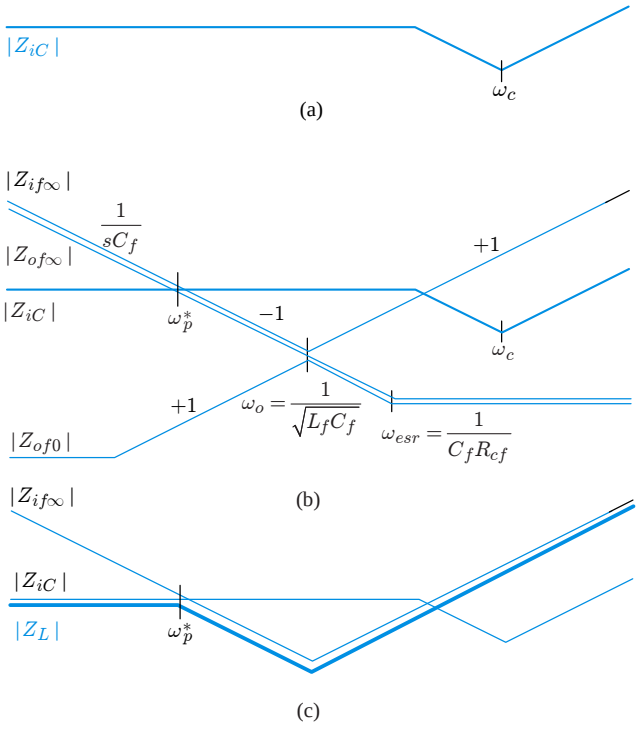


Figure 1.5 Asymptotic plots for various impedances. (a) Asymptotic plots for $|Z_{iC}|$. (b)Asymptotic plots for $|Z_{iC}|$, $|Z_{if\infty}|$, $|Z_{of\,0}|$, and $|Z_{of\,\infty}|$. (c) Construction of $|Z_L|$.

1) With the condition $|Z_{of0}| \ll |Z_{iC}|$ for all frequencies, the load impedance in (1.7) is simplified to

$$Z_L(s) = Z_{if\infty}\frac{1+\dfrac{Z_{of0}}{Z_{iC}(s)}}{1+\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \approx Z_{if\infty}\frac{1}{1+\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \tag{1.8}$$

2) For the frequencies where the condition $|Z_{of\infty}| \gg |Z_{iC}|$ is satisfied, the expression (1.8) is approximated as

$$Z_L(s) = Z_{if\infty}\frac{1}{1+\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \approx Z_{if\infty}\frac{1}{\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \tag{1.9}$$

which is further reduced to

$$Z_L(s) \approx Z_{iC}(s) \tag{1.10}$$

by noting that $|Z_{if\infty}| \approx |Z_{of\infty}|$ in the frequency range where $|Z_{of\infty}| \gg |Z_{iC}|$.

3) For the frequencies where the condition $|Z_{of\infty}| \ll |Z_{iC}|$ is met, the expression (1.8) is approximated as

$$Z_L(s) = Z_{if\infty}\frac{1}{1+\dfrac{Z_{of\infty}}{Z_{iC}(s)}} \approx Z_{if\infty} \tag{1.11}$$

The dividing line for the approximations of (1.10) and (1.11) occurs at the frequency labeled as ω_P^* in Fig. 1.5(b). By combining (1.10) and (1.11), it follows that

$$Z_L(s) \approx \begin{cases} Z_{iC}(s) : \text{for frequencies below } \omega_p^* \\ Z_{if\infty} : \text{for frequencies above } \omega_p^* \end{cases} \tag{1.12}$$

Figure 1.5(c) shows the construction of $|Z_L|$ using (1.12).

EXAMPLE 1.1 Filter Impedances and Load Impedance

This example shows the accuracy of the asymptotic analysis for $Z_L(s)$. Figure 1.6(a) shows the load subsystem used in this example. The Bode plots of $|Z_L|$, $|Z_{iC}|$, $|Z_{if\infty}|$, $|Z_{of0}|$, and $|Z_{of\infty}|$ of the load subsystem are shown in Figs. 1.6(b) and 1.6(c). A close resemblance between Fig. 1.5 and Fig. 1.6 confirms the accuracy of the preceding analysis.

1.1.3 Negative Resistance Approximation of $Z_{iC}(s)$

The previous analysis revealed the asymptotic behavior of the load impedance. At low frequencies, the load impedance follows the input impedance of the converter: $Z_L(s) \approx Z_{iC}(s)$. At mid and high frequencies, on the other hand, the load impedance tracks the open-circuit input impedance of the filter, $Z_L(s) \approx Z_{if\infty}$, which is determined with the condition that the converter stage is removed. This points out that the filter stage *masks* the mid- and high-frequency dynamics of the converter stage and the converter stage is only influential at low frequencies. Consequently, when analyzing the load impedance $Z_L(s)$, the low-frequency asymptote of $Z_{iC}(s)$ can be stretched for the entire frequency range and used as the replacement of the actual $Z_{iC}(s)$, without causing any noticeable error.

As will be demonstrated later, the input impedance of a regulated converter becomes a negative resistance at low frequencies, whose value is given by (1.1). For the load impedance evaluation, a regulated converter can thus be replaced with the negative resistance given by (1.1). The substitution of $Z_{iC}(s)$ by $-R_{iC}$ is referred to as the *negative resistance approximation* for $Z_{iC}(s)$.

The previous load impedance analysis in Fig. 1.2 adopted the negative resistance approximation. By comparing Fig. 1.2 and Fig. 1.5, it is clear that $|\omega_p| = \omega_p^* = 1/(C_f R_{iC})$.

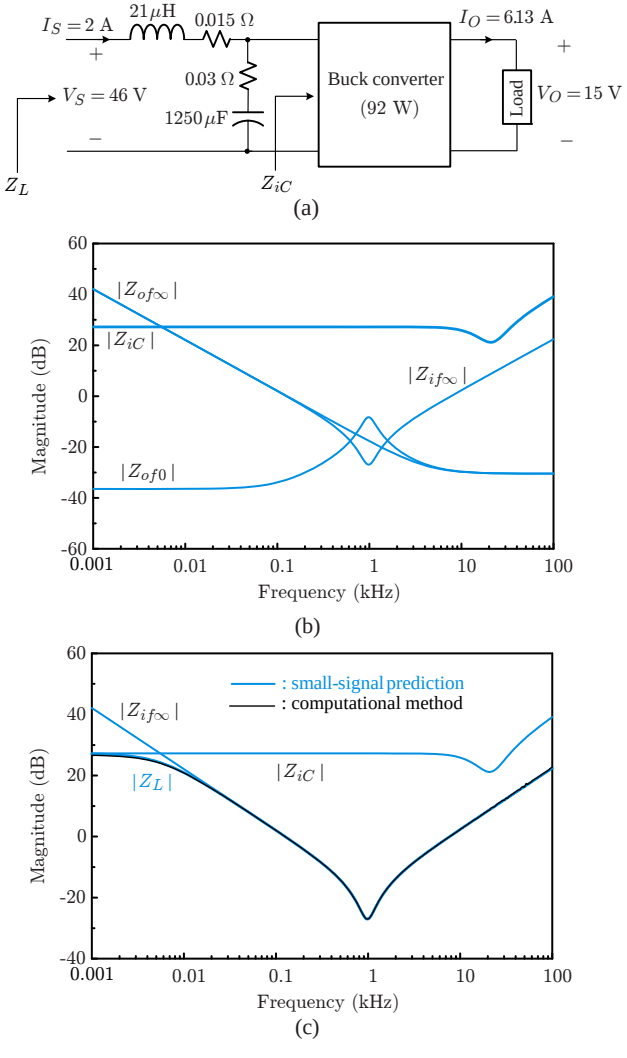


Figure 1.6 Bode plots of impedances. (a) Load subsystem. (b) Bode plots of $|Z_{iC}|$, $|Z_{if\infty}|$, $|Z_{of0}|$, and $|Z_{of\infty}|$. (c) Bode plots of $|Z_{iC}|$, $|Z_{if\infty}|$, and $|Z_L|$.

The conclusions of this section can be extended to include all general load subsystems. The negative resistance approximation for $Z_{iC}(s)$ is applicable to all converter topologies. Also, the construction procedure for the load impedance $Z_L(s)$ is valid for all other filter stage configurations combined with the negative resistance $-R_{iC}$.

Accuracy of Negative Resistance Approximation **EXAMPLE 1.2**

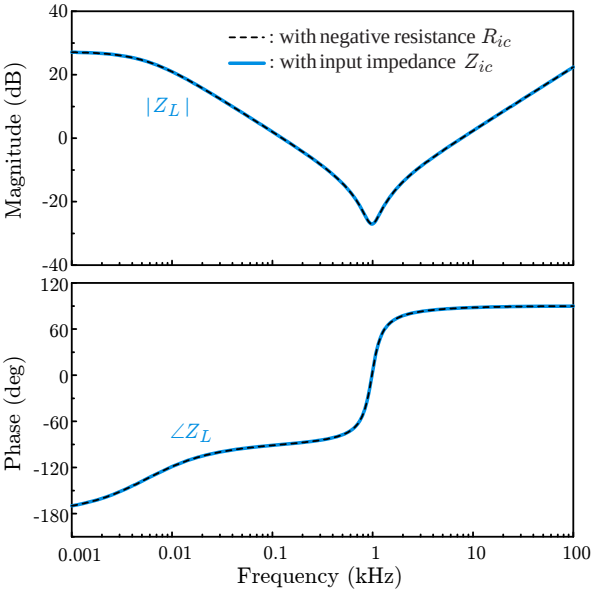


Figure 1.7 Accuracy of negative resistance approximation for $Z_L(s)$.

The accuracy of the negative resistance approximation for $Z_{iC}(s)$ is assessed in this example. Figure 1.7 compares the two different load impedances of the load subsystem used in Example 1.1. The first is evaluated using the exact input impedance of the regulated converter, $Z_{iC}(s)$, while the other is simulated using $-R_{iC}$ for $Z_{iC}(s)$. The two impedances are indistinguishable in both magnitude and phase characteristics.

1.2 STABILITY ANALYSIS OF LOAD-COUPLED CONVERTERS

Example **??** in the previous chapter demonstrated that the load impedance could markedly alter the performance of converters. Thus, the impacts of the load impedance have long been the subject of researches. The most important concern was whether a converter, which was stable under the uncoupled condition, could become unstable after being coupling with certain load impedances. If so, what types of the load impedance would destabilize a previously stable converter? If the converter remains stable, what changes will happen in the other performance criteria? We desire to answer these questions.

This section investigates the stability of the converter coupled with the load subsystem discussed in the previous section. An illustrative example is shown in Fig. 1.8. Stability can be analyzed using the loop gain of the load-coupled converter. Referring

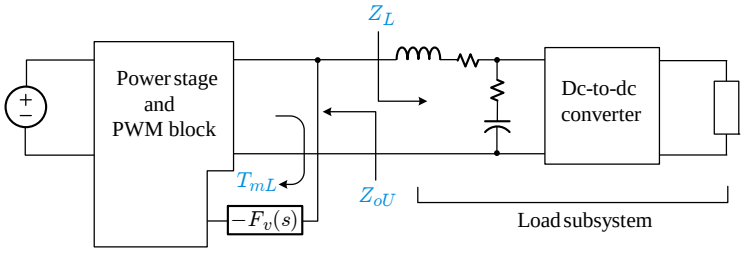


Figure 1.8 converter coupled with another converter via filter stage.

to Table 11.1, the loop gain of the load-coupled converter, $T_{mL}(s)$, is expressed as

$$T_{mL}(s) = \frac{T_{mU}(s)}{1 + \Big(1 + T_{mU}(s)\Big)\dfrac{Z_{oU}(s)}{Z_L(s)}} \tag{1.13}$$

where $T_{mU}(s)$ is the loop gain of the uncoupled converter, $Z_{oU}(s)$ is the output impedance of the uncoupled converter, and $Z_L(s)$ is the load impedance. Stability of the load-coupled converter is assessed using the characteristic equation

$$1 + T_{mL}(s) = 0 \tag{1.14}$$

which is given by

$$1 + \frac{T_{mU}(s)}{1 + \Big(1 + T_{mU}(s)\Big)\dfrac{Z_{oU}(s)}{Z_L(s)}} = 0 \tag{1.15}$$

The expression (1.15) is rearranged as

$$\Big(1 + T_{mU}(s)\Big)\left(1 + \frac{Z_{oU}(s)}{Z_L(s)}\right) = 0 \tag{1.16}$$

The solutions of this equation constitute the poles of the load-coupled converter.

The expression (1.16) reveals that the poles of the load-coupled converter are determined as the union of the poles of the uncoupled converter and the solutions of $1 + Z_{oU}(s)/Z_L(s) = 0$. It also indicates that the loading does not alter the existing poles of the uncoupled converter, but just creates new poles.

We assume the uncoupled converter is stable. Then, the stability of the load-coupled converter is decided by the solutions of $1+Z_{oU}(s)/Z_L(s) = 0$. Accordingly, the ratio $Z_{oU}(s)/Z_L(s)$ can be treated as a loop gain which determines stability of the load-coupled converter, as is the case with the *regular* loop gain $T_{mU}(s)$ of the uncoupled converter. In this perspective, the impedance ratio $Z_{oU}(s)/Z_L(s)$ is

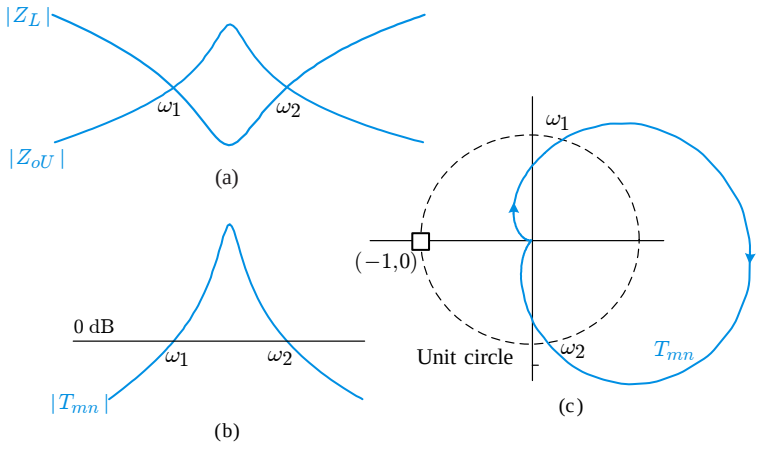


Figure 1.9 Bode plot and polar plot of impedance ratio Z_{oU}/Z_L as minor loop gain. (a) Bode plot of $|Z_{oU}|$ and Z_L. (b) Bode plot of $|T_{mn}|$. (c) Polar plot of T_{mn}.

defined as the *minor loop gain*[†]

$$T_{mn}(s) = \frac{Z_{oU}(s)}{Z_L(s)} \tag{1.17}$$

Now, the stability of the load-coupled converter is assessed from the solutions of $1 + T_{mn}(s) = 0$. The Nyquist criterion will be applied to $T_{mn}(s)$ to judge whether the load-coupled converter is stable or not. In addition, the phase margin and gain margin will be defined on $T_{mn}(s)$ to quantify the relative stability of the converter.

We illustrate the stability analysis using typical $Z_L(s)$ and $Z_{oU}(s)$ characteristics. Figure 1.9(a) depicts the Bode plots of $|Z_L|$ and $|Z_{oU}|$, which indicates that $|Z_{oU}|$ exceeds $|Z_L|$ in the frequency range of $\omega_1 < \omega < \omega_2$. Figure 1.9(b) is the Bode plot of $|T_{mn}| = |Z_{oU}|/|Z_L|$. For the frequencies where $|Z_{oU}| > |Z_L|$, $|T_{mn}|$ rises above the 0 dB line. Figure 1.9(c) displays the polar plot of $T_{mn}(s)$. The polar plot traces a closed path, starting from and returning to the origin, as the frequency ω increases from zero to infinity. In the frequency range of $\omega_1 < \omega < \omega_2$, where the $|T_{mn}|$ rises above the 0 dB line, the polar plot travels outside the unit circle.

1.2.1 Absolute Stability

The absolute stability of the load-coupled converter is determined by applying the Nyquist criterion to the polar plot trajectory of $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$. The converter becomes unstable when the polar plot trajectory encircles the $(-1, 0)$ point. Otherwise, the converter stands stable after loading. The illustrative polar plot in Fig. 1.9 is a stable case.

[†]The impedance ratio $Z_{oU}/Z_L(s)$ was originally termed as the minor loop gain in [2].

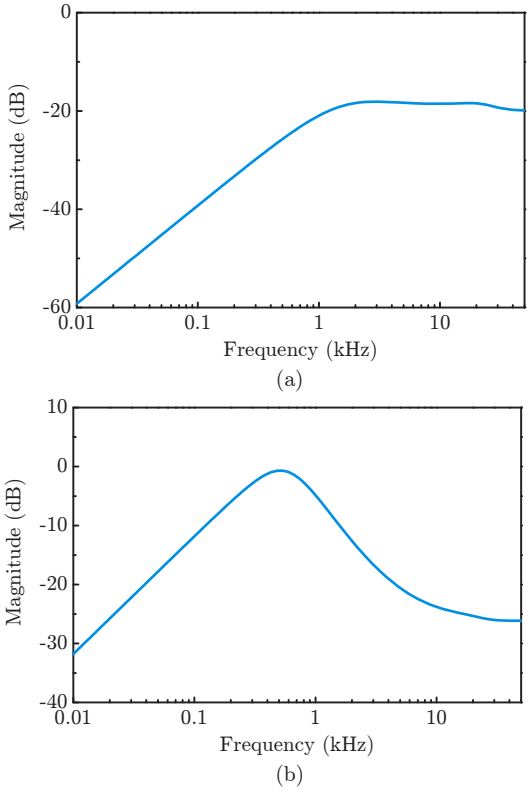


Figure 1.10 Output impedances of uncoupled converters. (a) Uncoupled buck converters. (b) Uncoupled boost converter.

As the first step of stability analysis, the discussions about $Z_L(s)$, $Z_{oU}(s)$, and $T_{mn}(s)$ need to be extended to general cases. The Bode plot of a typical $Z_L(s)$ was shown in Fig. **??**(c) and Fig. 1.7. The $Z_L(s)$ behaves as a negative resistance at low frequencies and exhibits a transitional dipping at mid frequencies. The phase of the load impedance varies between $-90^\circ < \angle Z_L < 90^\circ$ over the dipping.

The output impedance of the uncoupled converters, $Z_{oU}(s)$, was investigated in Chapter 5. The results of this analysis are repeated in Fig. 1.10, which shows the $Z_{oU}(s)$ of the buck converter in comparison of that of the boost converter. Figure 1.10 two different $Z_{oU}(s)$ patterns.

The $Z_{oU}(s)$ of the buck converter in Fig. 1.10(a) showed inductive characteristics at low frequencies and exhibited resistive behaviors at mid and high frequencies. This pattern of $Z_{oU}(s)$ is referred to as *Type A* output impedance. The $Z_{oU}(s)$ of the boost converter in Fig. 1.10(b) revealed a dissimilar pattern. The $Z_{oU}(s)$ undergoes a transitional peaking at mid frequencies before becoming resistive at high frequencies. The output impedance of this pattern is called *Type B* output impedance.

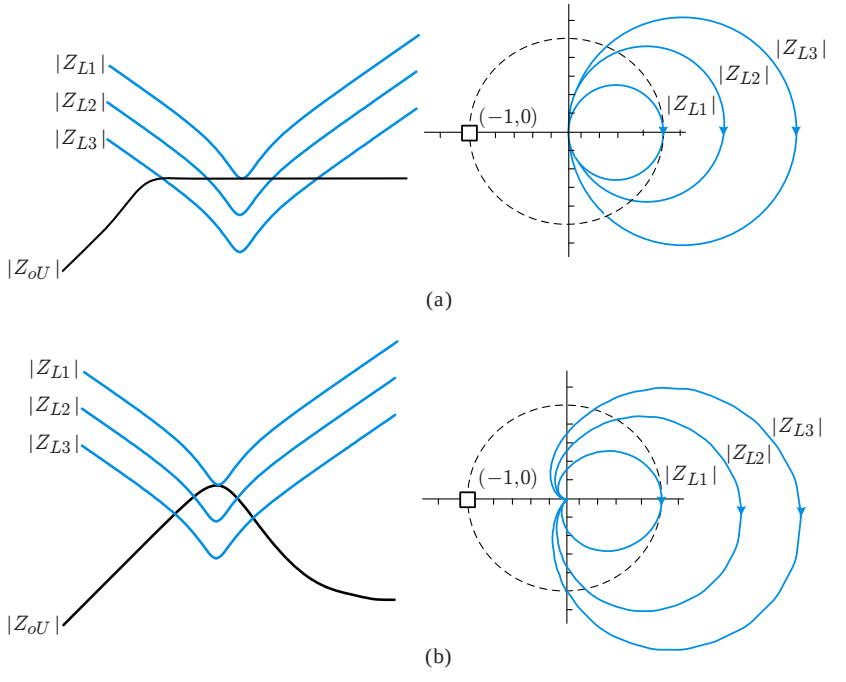


Figure 1.11 Bode plot and polar plot of minor loop gain (a) Type A output impedance case. (b) Type B impedance case.

Type A output impedance may occur in some buck converters in which the esr zero of the power stage transfer functions is located at sufficiently low frequencies. Type B output impedance is more common as it appears most cases of boost and buck/boost converters, and many cases of buck converters.

Figure 1.11 portraits the conceptual plots for the $|Z_{oU}|$ and $|Z_L|$, along with the polar plot trajectory of $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$. Figure 1.11(a) is the case where Type A output impedance is coupled with practical load subsystems, while Fig. 1.11(b) corresponds to the case of Type B output impedance. For each case, three different load impedances, $Z_{L1}(s)$, $Z_{L2}(s)$, and $Z_{L3}(s)$, are considered. The two cases both indicate that $|Z_{oU}|$ and $|Z_L|$ touch or overlap each other at the frequencies where $|Z_L|$ dips into the bottom value while $|Z_{oU}|$ attains its peak value.

The trajectories of the minor loop gain, $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$, are shown in the right-hand side in Fig. 1.11. The polar plots show different patterns in the two cases. The polar plot for the case of Type A output impedance is shown in 1.11(a). For this case, the phase of $T_{mn}(s)$, $\angle T_{mn} = \angle Z_{oU} - \angle Z_L$, changes between

$$0^\circ - (-90^\circ) > \angle T_{mn} > 0^\circ - (90^\circ) \quad \Rightarrow \quad 90^\circ > \angle T_{mn} > -90^\circ$$

because $\angle Z_{oU}$ stays at 0° while the phase of $Z_L(s)$ varies between $-90^\circ < \angle Z_L < 90^\circ$ over the impedance overlap. Accordingly, the polar plot always lies in the right-

half region of the s-plane, regardless of the magnitude of the impedance overlap, and never encircles the critical $(-1, 0)$ point. Consequently, the converter always maintains stability.

Figure 1.11(b) illustrates the Bode plots of $|Z_{oU}|$ and $|Z_L|$, together with the polar plot of $T_{mn}(s)$, for Type B output impedance case. The phase of $T_{mn}(s)$ alters between

$$90^\circ - (-90^\circ) > \angle T_{mn} > -90^\circ - (90^\circ) \quad \Rightarrow \quad 180^\circ > \angle T_{mn} > -180^\circ$$

because the phase of $Z_{oU}(s)$ varies between $90^\circ > \angle Z_{oU} > -90^\circ$ over the impedance overlap. For this case, the polar plot partially penetrates into the left-half region of the s-plain. As the overlap grows larger, the trajectory travels closer to the $(-1, 0)$ point. However, the polar plot never encircles the $(-1, 0)$ point because $\angle T_{mn}$ is bounded between $180^\circ > \angle T_{mn} > -180^\circ$. This indicates that the loading does not lead to instability.

The above argument is generalized in Fig. 1.12, which illustrates the impedance overlaps and polar plots of $T_{mn}(s)$ for four different cases. A typical $|Z_{oU}|$ of Type B is shown in Fig. 1.12. The phase of $Z_{oU}(s)$ starts from 90° at low frequencies, drops to -90° over the mid frequency peaking, and settles to 0° at high frequencies. On the other hand, the phase of the load impedance alters between $-90^\circ < \angle Z_L < 90^\circ$ over the impedance overlap. To predict the evolution of the polar plot trajectory, the boundaries of $\angle T_{mn} = \angle Z_{oU} - \angle Z_L$ are evaluated for the four different cases.

- Case A: $90^\circ - (-90^\circ) > \angle\,(Z_{oU}/Z_L) > 90^\circ - (90^\circ)$
  $\Rightarrow \quad 180^\circ > \angle\,(Z_{oU}/Z_L) > 0^\circ$
- Case B: $90^\circ - (-90^\circ) > \angle\,(Z_{oU}/Z_L) > -90^\circ - (90^\circ)$
  $\Rightarrow \quad 180^\circ > \angle\,(Z_{oU}/Z_L) > -180^\circ$
- Case C: $-90^\circ - (-90^\circ) > \angle\,(Z_{oU}/Z_L) > -90^\circ - (90^\circ)$
  $\Rightarrow \quad 0^\circ > \angle\,(Z_{oU}/Z_L) > -180^\circ$
- Case D: $0^\circ - (-90^\circ) > \angle\,(Z_{oU}/Z_L) > 0^\circ - (90^\circ)$
  $\Rightarrow \quad 90^\circ > \angle\,(Z_{oU}/Z_L) > -90^\circ$

The patterns of the polar plots are shown in Fig. 1.12. The polar plots do not encircle the $(-1, 0)$ point for all the four cases and the converter always stays stable. Here, it should be noted that the cases shown in Figs. 1.11 and 1.12 are based on the following assumptions.

- The loop gain of the uncoupled upstream converter has a sufficient phase margin so that $|Z_{oU}|$ does not show an excessive peaking.
- The filter stage in the load subsystem is well damped to avoid a large dipping

Now we are in the position to answer the question about the stability of the load-coupled converter. *Could certain load impedances destabilize the converter after loading*? For some cases, $|Z_L|$ is larger than $|Z_{oU}|$ for all frequencies, thereby initially precluding the possibility of any impedance overlap. The converter is invariably

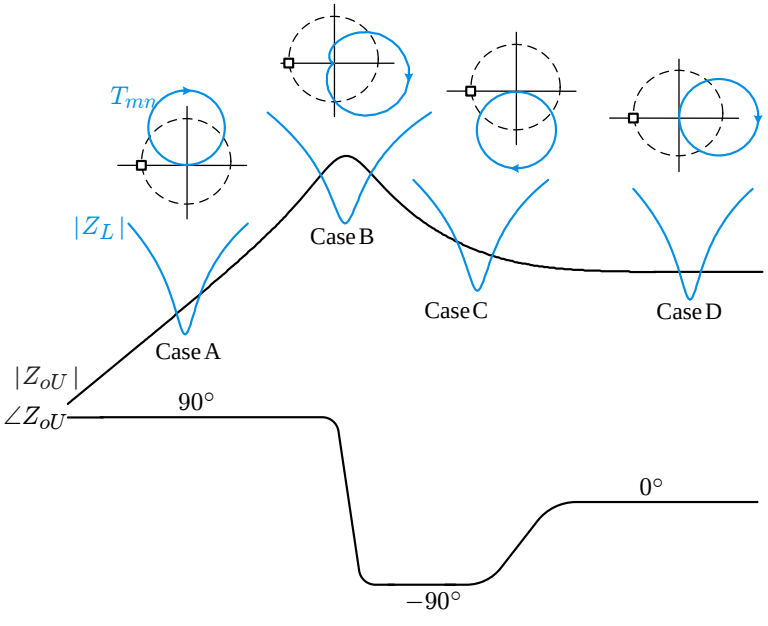


Figure 1.12 Impedance overlaps and polar plots of Z_{oU}/Z_L for general cases.

stable for this case. Actually, avoiding the overlap is the sufficient condition for stability. However, this sufficient condition rarely holds true in practice and the impedance overlap usually occurs after loading. Yet, for most practical cases, the overlap happens in the similar manner to those of Fig. 1.12. Therefore, the converter continues to be stable despite the presence of the impedance overlap, provided that the uncoupled converter secures a reasonable phase margin and the filter stage is adequately damped.

EXAMPLE 1.3 Stability Analysis of Load-Coupled Boost Converter

Illustrative examples are given in Fig. 1.13 to validate the preceding discussions. Figure 1.13(a) shows a load-coupled boost converter, where a current-mode controlled boost converter is integrated with a regulated buck converter through a filter stage. Both the boost converter and buck converter are designed based on standard design procedures. Figure 1.13(b) shows $|Z_{oU}|$ of the boost converter in comparison with the four different load impedances $|Z_L|$, Load A, Load B, Load C, and Load D. The load impedances are generated from the buck converter with four different sets of the filter parameters.

- **Load A:** $L_f = 210$ μH, $R_{lf} = 35$ mΩ, $C_f = 12500$ μF, and $R_{cf} = 10$ mΩ
- **Load B:** $L_f = 21$ μH, $R_{lf} = 15$ mΩ, $C_f = 1250$ μF, and $R_{cf} = 30$ mΩ

- **Load C:** $L_f = 2.1\ \mu$H, $R_{lf} = 10\ \text{m}\Omega$, $C_f = 125\ \mu$F, and $R_{cf} = 35\ \text{m}\Omega$
- **Load D:** $L_f = 2.1\ \mu$H, $R_{lf} = 10\ \text{m}\Omega$, $C_f = 10\ \mu$F, and $R_{cf} = 25\ \text{m}\Omega$

Figure 1.13(c) shows the polar plots of $T_{mn}(s)$ for the four different cases. As predicted, all the polar plots do not encircle $(-1, 0)$ point and the upstream boost converter stands stable after integration. The experimental verification of this analysis will be presented in a later section.

The previous analysis indicates that the converter remains stable after loading if the standard design procedures are exercised for both the converter stage and filter stage. Yet, the risk of instability still exists when a poorly-designed converter is coupled with an ill-conditioned load subsystem. A hypothetical example is shown in Fig. 1.14, where Type B output impedance is connected with certain load impedances. In this example, the impedance overlap happens at low frequencies where the load impedance behaves as a negative resistance, $-R_{iC}$. The phase of the load impedance is now fixed at $\angle Z_L = -180°$ and the phase of $T_{mn}(s)$ thus changes between

$$90° - (-180°) > \angle T_{mn} > -90° - (-180°) \quad \Rightarrow \quad 270° > \angle T_{mn} > 90°$$

The polar plot passes the $(-1, 0)$ point when $|Z_L|$ and $|Z_{oU}|$ touch each other and encircles the $(-1, 0)$ point when the two impedances overlap. These cases break the Nyquist criterion and lead to instability. The equation $1 + Z_{oU}(s)/Z_L(s) = 0$ finds two roots on the imaginary axis when the polar plot passes $(-1, 0)$ point. The two roots move into the right-half plane (RHP) of the s-plane when the polar plot encircles the $(-1, 0)$ point.

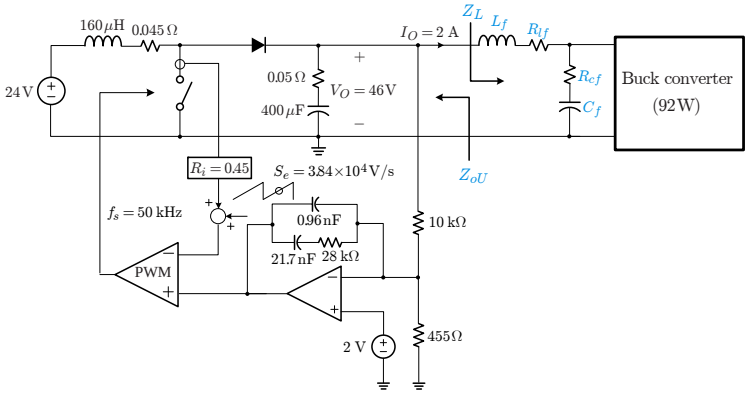
The unstable example in Fig. 1.14 is conceived under the following two assumptions.

1) The uncoupled converter produces the output impedance peaking at very low frequencies. This would happen only provided that the voltage feedback is improperly designed so that the loop gain crossover occurs at unusually low frequencies. When the standard design procedures are followed, the uncoupled converter rarely generates such a low-frequency output impedance peaking.

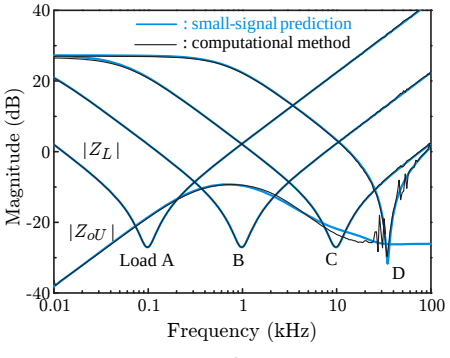
2) The parameters of the filter stage are uncommonly selected so that the load impedance shows a dipping at higher frequencies than normal cases. The resulting filter stage would not provide sufficient filtering and EMI standard won't be met.

The previous arguments insinuate that instability illustrated in Fig. 1.14 will not take place in practical applications.

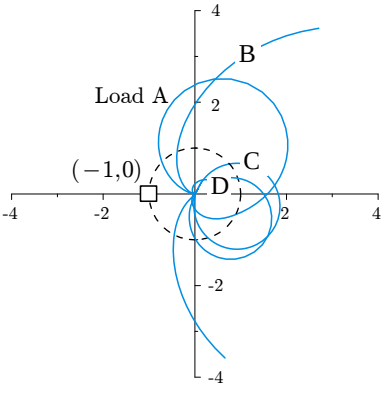
Another case of instability is depicted in Fig. 1.15. This example demonstrates the impacts of the filter stage on stability. Referring to Fig. 1.15(a), a filter stage is initially employed between the two converter stages. The impedance overlap between $|Z_{oU}|$ and $|Z_L|$ and $T_{mn}(s)$ trajectory are shown with thin lines in Figs. 1.15(b) and 1.15(c). Stability is confirmed from the $T_{mn}(s)$ trajectory. Now, the filter



(a)



(b)



(c)

Figure 1.13 Stability analysis of load-coupled boost converter. (a) Boost converter feeding buck converter via filter stage. (b) Load impedances $|Z_L|$ and output impedance of uncoupled converter $|Z_{oU}|$. (c) Polar plots of minor loop gain.

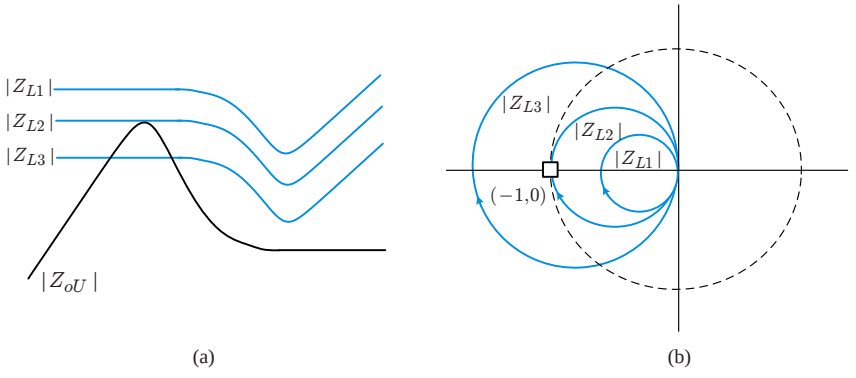


Figure 1.14 Hypothetical example of instability. (a) Bode plot of $|Z_{oU}|$ and $|Z_L|$. (b) Polar plot of Z_{oU}/Z_L.

stage is removed and the upstream converter is directly connected to the downstream converter. The load impedance and the minor loop gain at the absence of the filter stage, denoted as $Z'_L(s)$ and $T'_{mn}(s)$ in Fig. 1.15, are shown with thick lines. The polar plot violates the Nyquist criterion and the system loses stability.

The filter stage is primarily employed for filtering, yet it also plays an important role in the system stability. *The filter stage prevents potential instability by masking the negative input resistance of the regulated converter at the frequencies of impedance overlap.* Thus, the filter stage is essential not only for the filtering but the system stability as well.

Instability at Absence of Filter Stage — EXAMPLE 1.4

Instability described in Fig. 1.15 is exemplified in Fig. 1.16. Figure 1.16(a) shows a boost converter coupled with a load subsystem. The load subsystem is normally designed. However, the control parameters of the upstream boost converter are deliberately selected so that $|Z_{oU}|$ produces a large peaking. Figure 1.16(b) shows $|Z_{oU}|$ in comparison with the load impedance with the filter stage, $|Z_L|$, and magnitude of the load impedance without the filter stage, $|Z'_L|$. The polar plots of the two different minor loop gains, $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$ with the filter stage and $T'_{mn}(s) = Z_{oU}(s)/Z'_L(s)$ without the filter stage, are shown in Fig. 1.16(c). The polar plot of $T'_{mn}(s)$ encircles the $(-1, 0)$ point thus predicting instability at the absence of the filter stage.

Figure 1.16(d) is the output voltage waveform of the boost converter, going through the transition from the stable to unstable operations. Initially, the filter stage was employed to produce a stable output voltage. In the middle of the stable operation, the filter stage is removed and the boost converter is directly connected to the buck converter. As predicted, the output voltage develops a growing oscillation, as a token of instability.

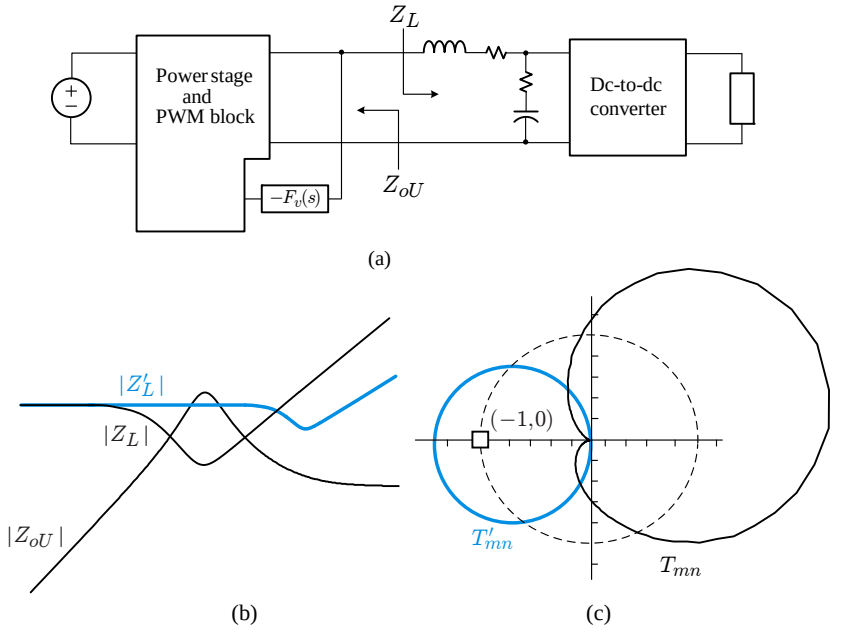


Figure 1.15 Impacts of filter stage on system stability. (a) System block diagram. (b) Bode plot of $|Z_{oU}|$ and Z_L. (b) Polar plot of T_{mn}.

Concluding Summary:

Load-coupled converters become unstable only provided that the impedance overlap happens at the frequencies where the load impedance behaves as a negative resistance. converters coupled with general linear loads, not presenting the negative resistance, shall maintain stability, regardless of the extent and the frequency range of the impedance overlap.

Regulated converters, presenting a negative resistance at low frequencies, are the prime source of instability. Even for these cases, instability can readily be prevented by avoiding the impedance overlap at low frequencies. In fact, the low-frequency impedance overlap rarely occurs in practice when converters and filter stages are properly designed.

The loading in general will not make the converter unstable. Nonetheless, the loading could deteriorate other performance of the converter. The loading could induce a peaking in frequency responses or make the transient responses oscillatory or sluggish. The loading effects on the converter performance will be treated later in detail.

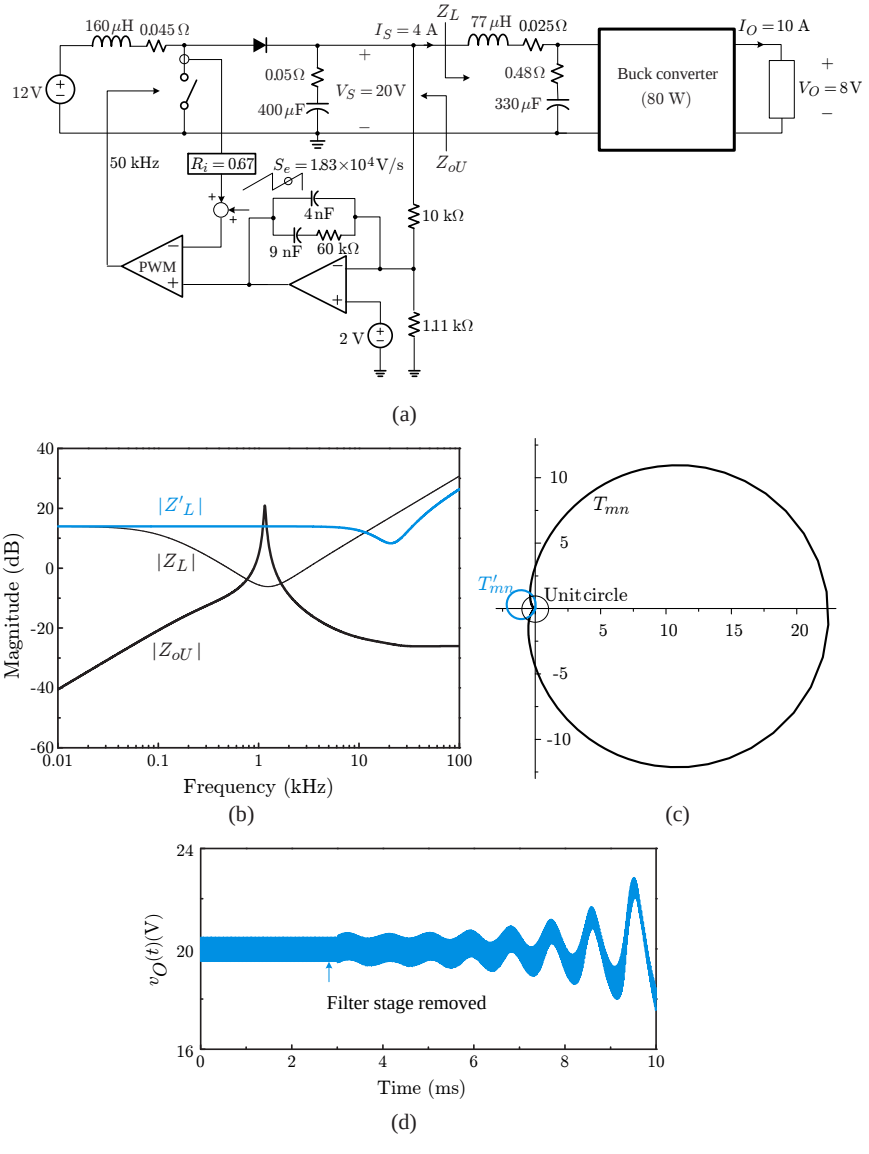


Figure 1.16 Instability at absence of filter stage. (a) Dc power conversion system. (b) Bode plots of $|Z_{oU}|$, $|Z_L|$, and $|Z'_L|$. (c) Polar plots of T_{mn} and T'_{mn}. (d) Output voltage waveform of boost converter.

1.2.2 Relative Stability

The characteristic equation of the load-coupled converter is given by

$$\left(1 + T_{mU}(s)\right)\left(1 + \frac{Z_{oU}(s)}{Z_L(s)}\right) = 0 \tag{1.18}$$

The impedance ratio $Z_{oU}(s)/Z_L(s)$, defined as the minor loop gain $T_{mn}(s)$, was used to judge the absolute stability. Now, the minor loop gain is employed to quantify the relative stability of the converter, as is the case with the regular loop gain $T_{mU}(s)$. The phase margin and gain margin are defined on $T_{mn}(s)$ as follows.

Phase Margin: Referring to Fig. 1.17, two different phase margins are defined at the two distinct frequencies, ω_1 and ω_2, where the polar plot crosses the unit circle, or equivalently $|T_{mn}|$ passes the 0 dB line

- Phase margin at ω_1: $\mathrm{PM}_1 = 180^\circ - \angle T_{mn}(j\omega_1)$
- Phase margin at ω_2: $\mathrm{PM}_2 = \angle T_{mn}(j\omega_2) - (-180^\circ)$

Figure 1.17(a) depicts the phase margins on the polar plot, while Fig. 1.17(b) portraits the phase margins on the Bode plot.

Gain Margin: The gain margin is defined at the frequency ω_0 where the polar plot crosses the $-$ real axis, or equivalently $\angle T_{mn}$ falls to 180°. When the polar plot crosses the $(-k, 0)$ point, the gain margin is given by $\mathrm{GM} = 20\log(1/k)$. The gain margin is illustrated in Figs. 1.17(a) and 1.17(b).

The phase and gain margins specify the additional phase change and magnitude increase that can be added to $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$ before the converter encounters instability. More importantly, the stability margins serve as a gauge for the closed-loop performance of the converter. In particular, a small phase margin is an indication of peaking in transfer functions and oscillatory behaviors in transient responses. Details about this topic will be given in a later section.

Most significantly, the stability margins of the minor loop gain usually become the stability margins of the loop gain of the load-coupled converter. For example, the phase margin PM_1, defined for the minor loop gain in Fig. 1.17, becomes the phase margin of the loop gain of the load-coupled converter. The proof of this rather surprising fact will be given in the next section.

EXAMPLE 1.5 Minor loop gain $T_{mn}(s)$ and phase margins

This example shows the impedance overlap, polar plot, and Bode plot of the minor loop gain $T_{mn}(s)$ of the dc power conversion system shown in Fig. 1.18(a). Figure 1.18(b) displays the impedance overlap between $Z_{oU}(s)$ and $Z_L(s)$. The polar plot and Bode plot of the minor loop gain, $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$, are shown in Fig. 1.18(c). The phase margins of $T_{mn}(s)$ are determined as $\mathrm{PM}_1 = 62^\circ$ at $\omega_1 = 2\pi \cdot 300$ rad/s and $\mathrm{PM}_2 = 60^\circ$ at $\omega_2 = 2\pi \cdot 2.2 \times 10^3$ rad/s.

1.3 LOOP GAIN ANALYSIS OF LOAD-COUPLED CONVERTERS

The load subsystem seldom destabilizes a previously stable upstream converter. However, the load impedance usually induces significant changes in the converter

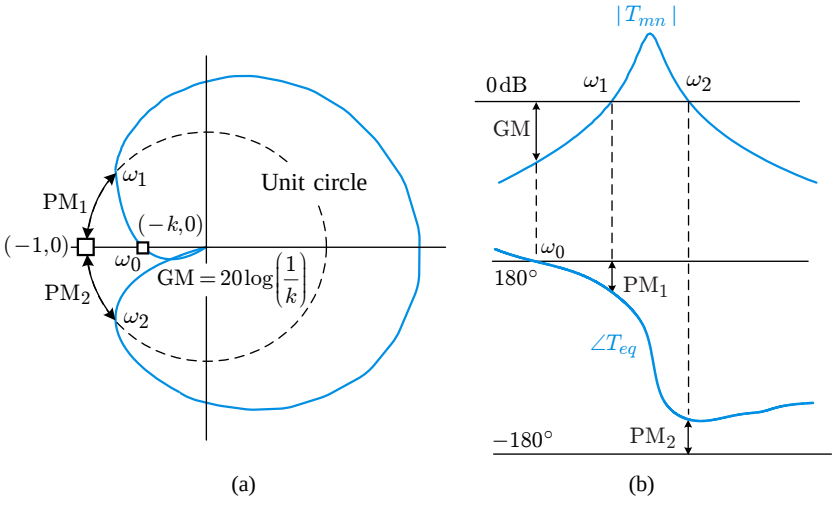


Figure 1.17 Phase margin and gain margin of minor loop gain. (a) Polar plot representation. (b) Bode plot representation.

dynamics, yielding very complex loop gain characteristics. This section investigates the loop gain of the load-coupled converter, focusing on the impacts of the load subsystem.

1.3.1 Graphical Analysis and Construction of $T_{mL}(s)$

The loop gain expression in (1.13) can be modified as

$$T_{mL}(s) = \frac{T_{mU}(s)}{1+\Big(1+T_{mU}(s)\Big)\dfrac{Z_{oU}(s)}{Z_L(s)}} = \frac{T_{mU}(s)}{1+\Big(1+T_{mU}(s)\Big)T_{mn}(s)}$$

$$= \boxed{\frac{T_{mU}(s)}{1+T_{mn}(s)+T_{mU}(s)T_{mn}(s)}} \tag{1.19}$$

where $T_{mU}(s)$ is the loop gain of the uncoupled converter and $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$ is the minor loop gain. The converter loop gain will be unaffected, $T_{mL}(s) \approx T_{mU}(s)$, when the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$ are simultaneously met. However, this requirement is usually not satisfied and the loop gain characteristics are thus to be altered by $Z_L(s)$. The expression (1.19) is used to characterize and construct the loop gain of the load-coupled converter.

Figure 1.19 shows the construction of the converter loop gain $|T_{mL}|$ based on (1.19). The following assumptions are made to simplify the $|T_{mL}|$ construction.

1) The loop gain of the uncoupled converter, $|T_{mU}|$, has an integrator structure and crosses the 0 dB line at ω_c with a phase margin of PM_c.

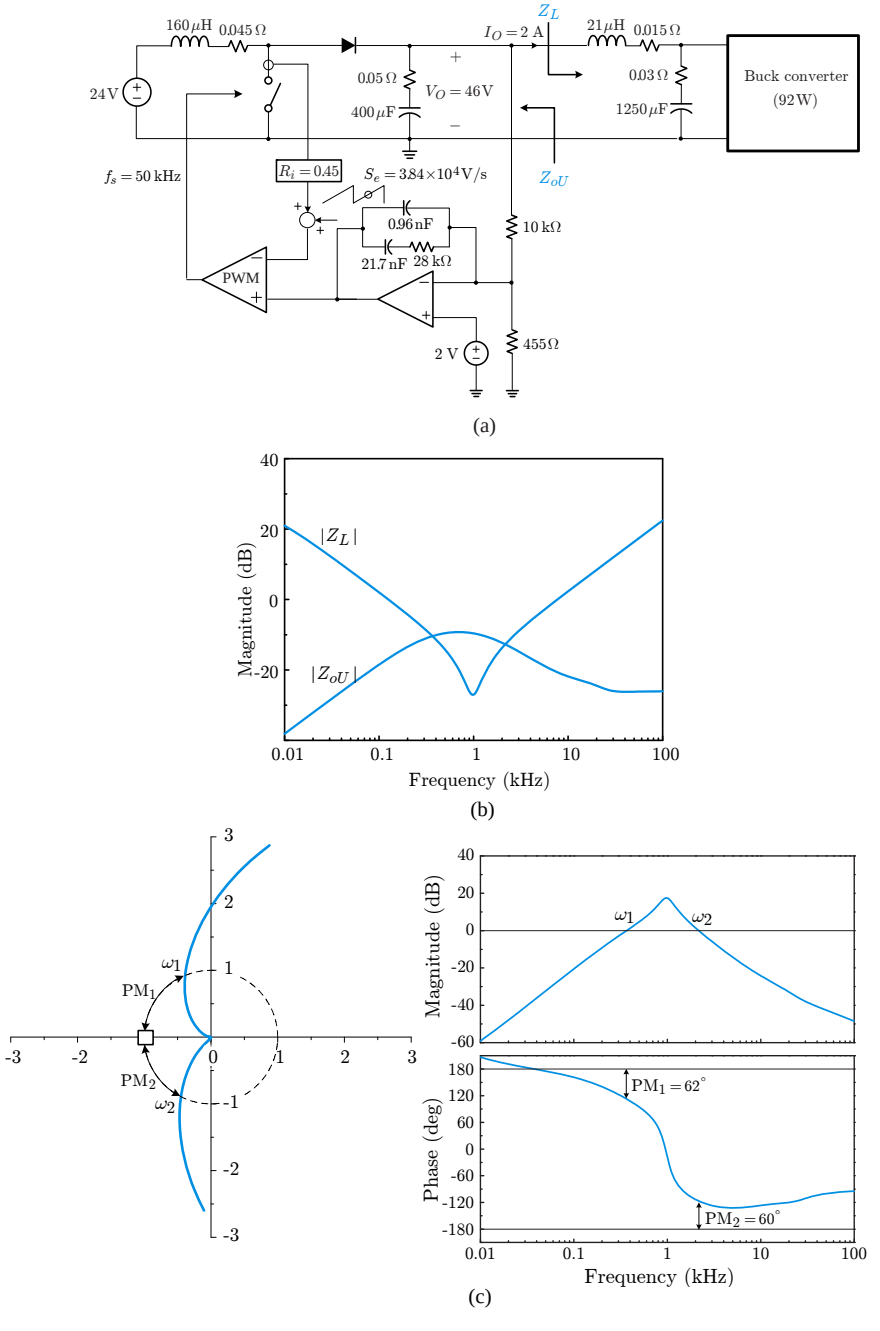


Figure 1.18 Phase margin of minor loop gain of dc power conversion system. (a) Dc power conversion system. (b) Bode plot of Z_{oU} and Z_L. (c) Phase margins of minor loop gain.

2) The minor loop gain, $|T_{mn}| = |Z_{oU}/Z_L|$, crosses the 0 dB line at ω_1 and ω_2 with the respective phase margin of PM_1 and PM_2.

In Fig. 1.19, the asymptotic plot for $|T_{mU}\, T_{mn}|$ is drawn by adding $|T_{mU}|$ and $|T_{mn}|$. As shown in Fig. 1.19, the construction of $|T_{mL}|$ is classified into the three cases, based on the locations of the crossover frequencies of $|T_{mU}|$ and $|T_{mn}|$.

Case A: Shown in Fig. 1.19(a) is Case A, where the crossover frequencies of $|T_{mn}|$ come earlier than the crossover frequency of $|T_{mU}|$, $\omega_1 < \omega_2 < \omega_c$. Up to the frequency where $|T_{mU}\, T_{mn}|$ crosses the 0 dB line, denoted as ω_c' in Fig. 1.19(a), the conditions $1 \ll |T_{mU}\, T_{mn}|$ and $|T_{mn}| \ll |T_{mU}\, T_{mn}|$ prevail. Thus, for the frequencies below ω_c', the loop gain is given by

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mU}(s)}{1 + T_{mn}(s) + T_{mU}(s)T_{mn}(s)} \\ &\approx \frac{T_{mU}(s)}{T_{mn}(s) + T_{mU}(s)T_{mn}(s)} \approx \frac{T_{mU}(s)}{T_{mU}(s)T_{mn}(s)} = \frac{1}{T_{mn}(s)} \end{aligned}$$

Thus, $|T_{mL}|$ follows the mirror image of $|T_{mn}|$ reflected on the 0 dB axis, as highlighted with thick lines in blue in Fig. 1.19(a). For the frequencies beyond ω_c' where the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$ are met, the loop gain of the load-coupled converter trails the loop gain of the uncoupled converter, $T_{mL}(s) \approx T_{mU}(s)$. A peaking may occur at ω_c' where $|T_{mL}|$ diverts from $1/|T_{mn}|$ to $|T_{mU}|$, as shown in Fig. 1.19(a).

The $|T_{mL}|$ exhibits very involved characteristics, even crossing the 0 dB line three times. However, the converter remains stable as far as $T_{mn}(s)$ meets the Nyquist stability criterion. With multiple 0 dB crossovers, the phase margin is not uniquely determined for this case.

Case B: Figure 1.19(b) shows Case B, where the crossover frequency of $|T_{mU}|$ appears between the crossover frequencies of $|T_{mn}|$, $\omega_1 < \omega_c < \omega_2$. For the frequencies below ω_c where the conditions $1 \ll |T_{mU}\, T_{mn}|$ and $|T_{mn}| \ll |T_{mU}\, T_{mn}|$ hold, $|T_{mL}|$ follows $1/|T_{mn}|$, as is the previous case. On the other hand, the conditions $1 \ll |T_{mn}|$ and $|T_{mU}\, T_{mn}| \ll |T_{mn}|$ are valid in the frequency range of $\omega_c < \omega < \omega_2$. These conditions simplify loop gain expression to

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mU}(s)}{1 + T_{mn}(s) + T_{mU}(s)T_{mn}(s)} \\ &\approx \frac{T_{mU}(s)}{T_{mn}(s) + T_{mU}(s)T_{mn}(s)} \approx \frac{T_{mU}(s)}{T_{mn}(s)} \end{aligned}$$

This indicates that, in the frequency range of $\omega_c < \omega < \omega_2$, the loop gain magnitude is formed by the relationship of $|T_{mL}| = |T_{mU}| - |T_{mn}|$. At the frequencies after ω_2, $|T_{mL}|$ tracks $|T_{mU}|$ with the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$. A peaking could appear at the second crossover frequency of $|T_{mn}|$, ω_2. The magnitude of the peaking is inversely proportional to the phase margin of $|T_{mn}|$ at ω_2, PM_2.

Table 1.1 Summary of Loop Gain Analysis

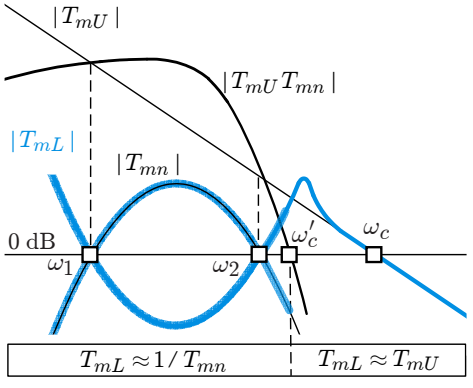
	T_{mL} from low to mid frequencies	0 dB crossover frequency of T_{mL}	Phase margin of T_{mL}
Case A $\omega_1 < \omega_2 < \omega_c$	$T_{mL} = \dfrac{1}{T_{mn}}$	$\omega_1, \omega_2,$ and ω_c	Not uniquely defined
Case B $\omega_1 < \omega_c < \omega_2$	$T_{mL} = \dfrac{1}{T_{mn}}$	ω_1	PM_1
Case C $\omega_c < \omega_1 < \omega_2$	$T_{mL} = T_{mU}$	ω_c	PM_c

As shown in Fig. 1.19(b), the crossover frequency of $|T_{mL}|$ occurs at ω_1 which is the first crossover frequency of $|T_{mn}|$. At the frequencies around ω_1, $T_{mL}(s)$ is given by the inverse of $T_{mn}(s)$: $T_{mL}(s) = 1/T_{mn}(s)$. *This implies the phase margin of $T_{mL}(s)$ is the same as the phase margin of $T_{mn}(s)$.* The sameness of the phase margin is illustrated in Fig. 1.20 with a simple example. Figure 1.20(a) shows the Bode plot of $T_{mn}(s)$ and $1/T_{mn}(s)$, where $T_{mn}(s)$ is selected as $T_{mn}(s) = 7148/(s(1 + s/5000))$. The Bode plots are converted into the polar plots in Fig. 1.20(b) to show the phase margins are identical.

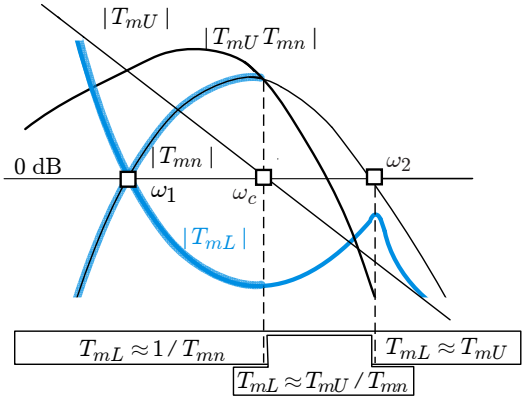
Case C: Figure 1.19(c) displays Case C with $\omega_c < \omega_1 < \omega_2$. The $|T_{mL}|$ largely trails $|T_{mU}|$, except for the frequency range of $\omega_1 < \omega < \omega_2$, where $|T_{mL}|$ tracks $|T_{mU}/T_{mn}|$ due to the conditions $1 \ll |T_{mn}|$ and $|T_{mU}T_{mn}| \ll |T_{mn}|$. The crossover frequency and phase margin of the load-coupled converter are the same as those of the uncoupled converter, because the load impedance is only effective after the crossover frequency of $T_{mU}(s)$.

The outcomes of the preceding loop gain analysis are summed up in Table 1.1. Among the three cases, Case B will occur most frequently for the following reasons. The peaking in $|Z_{oU}|$ usually appears at the crossover frequency of $|T_{mU}|$. On the other hand, the impedance overlap typically takes place over the frequencies at which $|Z_{oU}|$ reaches its peak. Therefore, the crossover frequency of $|T_{mU}|$ lies inside the frequency range of the impedance overlap – Case B in Fig. 1.19.

For Case B, the crossover frequency and phase margin of $T_{mL}(s)$ are determined by those of the minor loop gain $T_{mn}(s)$. This indicates that, although the loop gain is substantially altered over a wide frequency range, the converter remains stable as far as $T_{mn}(s)$ meets the Nyquist stability criterion. Furthermore, the converter retains good transient responses unless the phase margin and the crossover frequency of $T_{mn}(s)$ are unduly small and narrow.



(a)



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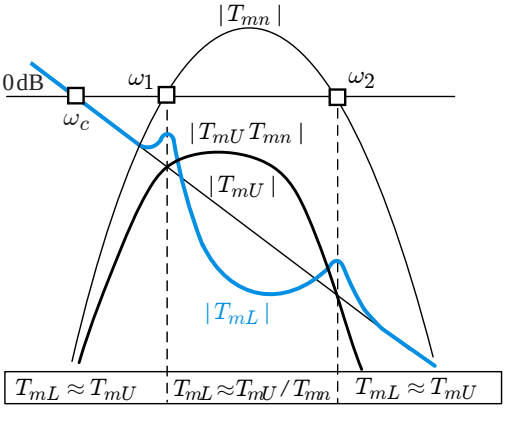


(c)

Figure 1.19 Construction of loop gain of load-coupled converter. (a) Case A: $\omega_1 < \omega_2 < \omega_c$. (b) Case B: $\omega_1 < \omega_c < \omega_2$. (c) Case C: $\omega_c < \omega_1 < \omega_2$.

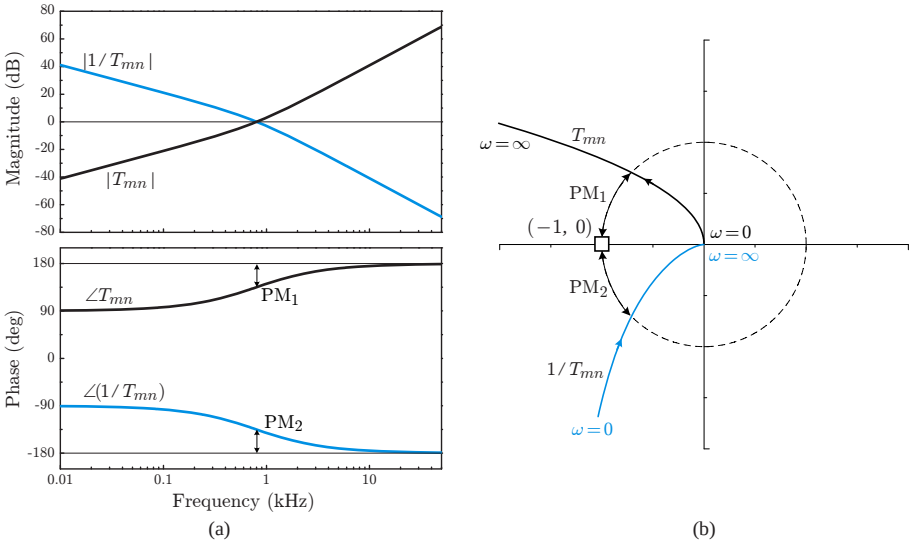


Figure 1.20 Bode and polar plots of T_{mn} and $1/T_{mn}$. (a) Bode plots. (b) Polar plots.

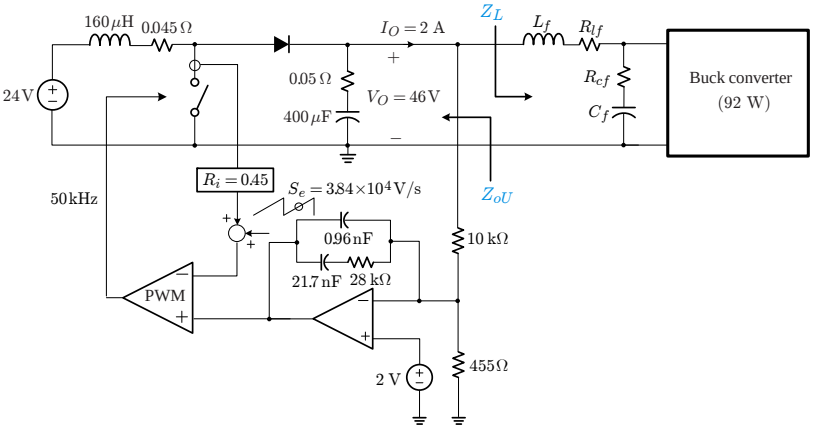


Figure 1.21 Dc power conversion system.

EXAMPLE 1.6 Loop Gain Analysis of Load-Coupled Boost Converter

This example validates the preceding loop gain analysis. Figure 1.21 is the dc power conversion system employed in this example. Figure 1.22(a) shows the load impedance $|Z_L|$ of the three different load subsystems, together with the output impedance of the uncoupled boost converter, $|Z_{oU}|$. Each load subsystem contains an identical buck converter in common, yet has unequal circuit parameters for the filter stage

- Load A: $L_f = 210\ \mu$H, $R_{lf} = 35\ \text{m}\Omega$, $C_f = 12500\ \mu$F, and $R_{cf} = 10\ \text{m}\Omega$
- Load B: $L_f = 21\ \mu$H, $R_{lf} = 15\ \text{m}\Omega$, $C_f = 1250\ \mu$F, and $R_{cf} = 30\ \text{m}\Omega$
- Load C: $L_f = 2.1\ \mu$H, $R_{lf} = 10\ \text{m}\Omega$, $C_f = 125\ \mu$F, and $R_{cf} = 35\ \text{m}\Omega$

As shown in Fig. 1.22(b), the three load subsystems produce Case A, Case B, and Case C, covered in the previous analysis. Figure 1.22(c) shows the loop gains of the boost converter coupled with each load subsystem. The loop gain exhibits substantial changes after coupling with Load A and Load B.

Figure 1.22(d) displays the simulation results for Load A, which reveals a close agreement with the asymptotic analysis for Case A in Fig. 1.19(a). Figure 1.22(e) is the results for Load B, which corresponds to Case B in Fig. 1.19(b). The simulation results of Load C, or Case C, are displayed in Fig. 1.22(f).

Verification of Converter Performance for Case B **EXAMPLE 1.7**

The dc power conversion system used in the previous analyses was built. The loop gain and step load response of the boost converter were then measured with Load B. The same experiments were performed after replacing Load B with a current sink. Figure 1.23(a) shows the measured loop gains of the load-coupled boost converter, $T_{mL}(s)$, and uncoupled boost converter, $T_{mU}(s)$, along with the small-signal simulation results. Close correlations between the experimental measurements and analytical predictions support the validity and accuracy of the analyses.

Figure 1.23(b) exhibits the transient responses of the uncoupled and load-coupled converters. The upper traces show the output voltage, $v_O(t)$, and inductor current, $i_L(t)$, of the boost converter connected with a current sink load, in response to $2\,\text{A} \Rightarrow 1.5\,\text{A} \Rightarrow 2\,\text{A}$ changes in the sink current. The lower traces are the waveforms of the boost converter connected with Load B, where $92\,\text{W} \Rightarrow 69\,\text{W} \Rightarrow 92\,\text{W}$ power changes are introduced to the buck converter downstream. The loading makes the transient response somewhat oscillatory and sluggish. Nonetheless, the converter retains stability and performance after loading. Detailed discussions about the loading effects on the transient response will be given in the next section.

Finally, Fig. 1.23(c) illustrates the minor loop gain for Load B. The crossover frequency and phase margin of the minor loop gain are the same as those of the loop gain of the boost converter integrated with the load subsystem.

1.3.2 Conditions for *Unaffected* Loop Gain Characteristics

It is instructive to identify the conditions that prevent the loop gain from being affected by loading. Referring to the expression in (1.19), the loop gain stands unaffected when the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \ll 1$ are met for the entire frequency range.

Although the first condition $|T_{mn}| \ll 1$ might be met for all frequencies, the second requirement $|T_{mU}T_{mn}| \ll 1$ is usually violated at low frequencies because $|T_{mU}|$ becomes increasingly larger at lower frequencies. Thus, the low-frequency loop gain characteristics are invariably altered by loading. However, if the condition

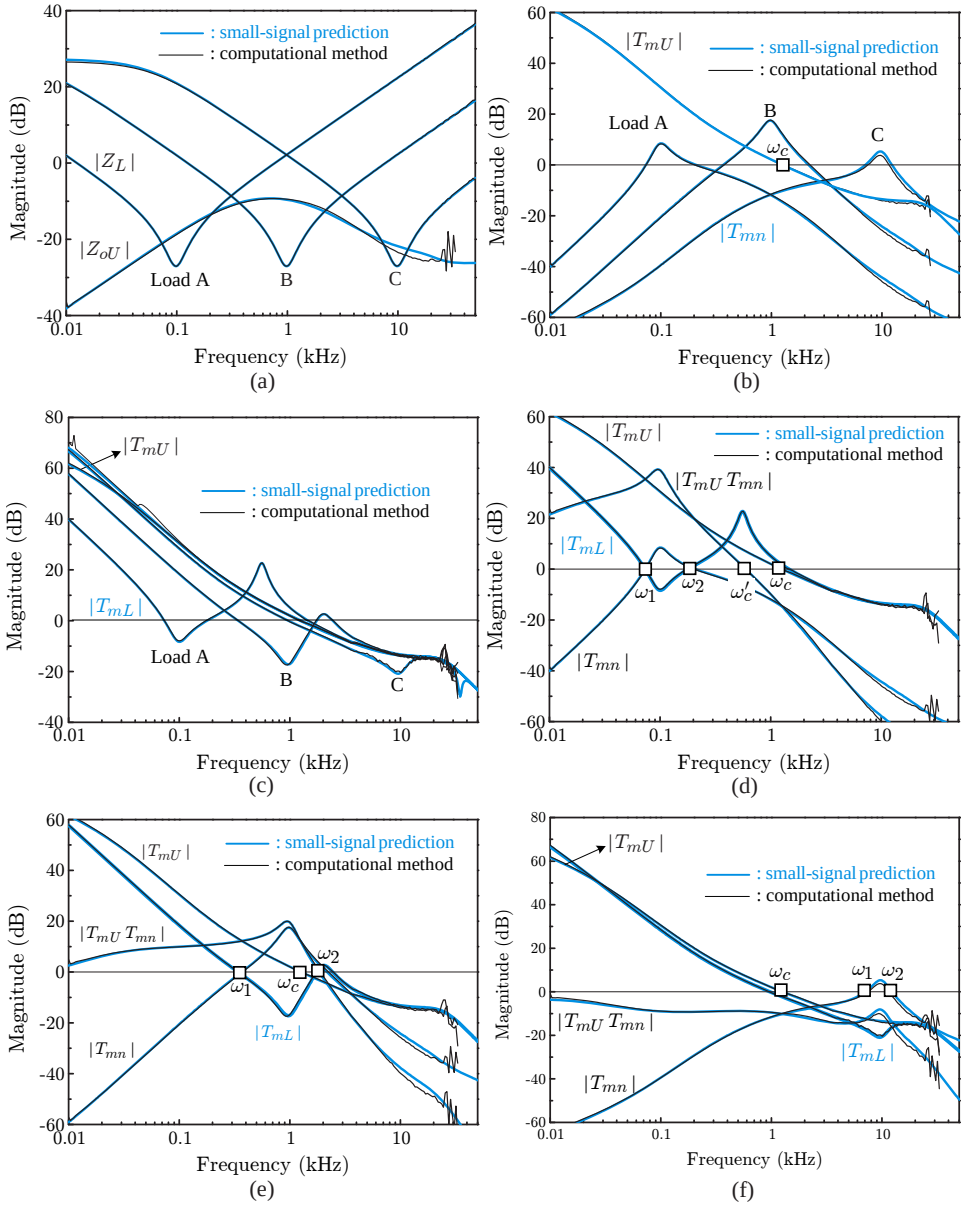


Figure 1.22 Loop gain analysis of dc power conversion system. (a) Load impedances. (b) minor loop gains. (c) Loop gains of boost converter. (d) Loop gain analysis for Case A. (e) Loop gain analysis for Case B. (f) Loop gain analysis for Case C.

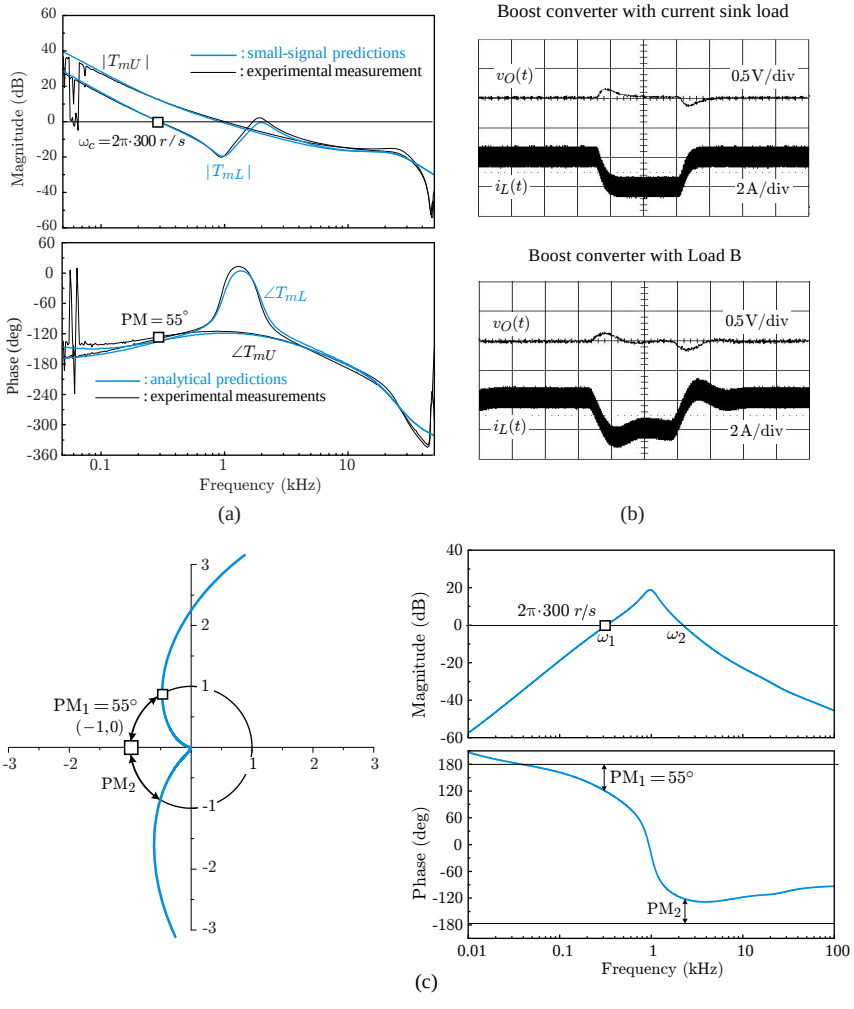
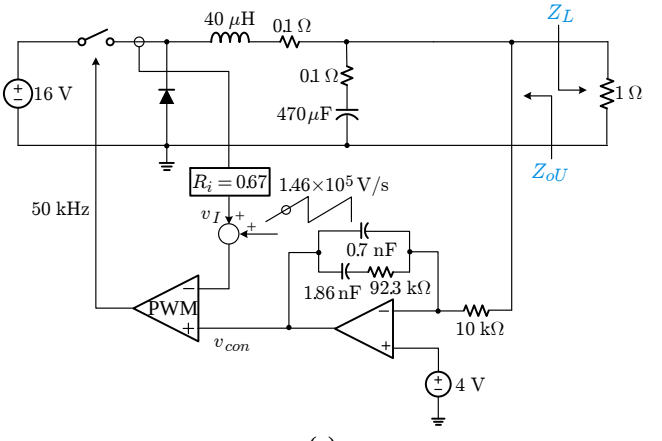


Figure 1.23 Experimental verification of converter performance for Case B. (a) Loop gain. (b) Step load response. (c) minor loop gain.

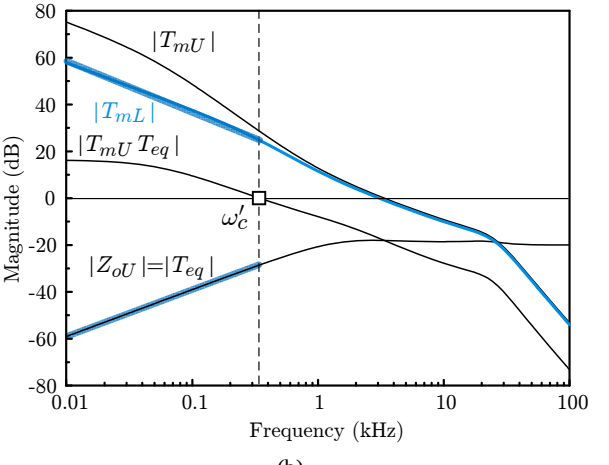
$|T_{mn}| \ll 1$ is met for all frequencies, the change only occurs in the frequencies well below the loop gain crossover frequency, thereby not affecting stability and performance of the load-coupled converter.

Resistor-Coupled Buck Converter Case — EXAMPLE 1.8

This example deals with the loop gain analysis of a buck converter connected to a resistive load. Figure 1.24(a) shows the buck converter considered in this example. This converter was used in Examples **??** through **??** in Chapter 4.



(a)



(b)

Figure 1.24 Loop gain analysis of resistor-loaded buck converter. (a) Circuit diagram. (b) Loop gain analysis.

The buck converter is loaded with a 1 Ω resistor. Accordingly, $Z_L(s) = 1$ and $Z_{oU}(s)$ itself is the minor loop gain, $T_{mn}(s) = Z_{oU}(s)/Z_L(s) = Z_{oU}(s)$. Figure 1.24(b) shows $|T_{mn}|$, $|T_{mU}|$, $|T_{mU}T_{mn}|$, and $|T_{mL}|$. The condition $|T_{mn}| \ll 1$ is well satisfied for all frequencies. However, $1 \gg |T_{mU}T_{mn}|$ is not met at low frequencies. For the frequencies below ω_c' where the conditions $|T_{mn}| \ll 1$ and $|T_{mU}T_{mn}| \gg 1$ prevail, the loop gain is given by

$$T_{mL}(s) = \frac{T_{mU}(s)}{1 + T_{mn}(s) + T_{mU}(s)T_{mn}(s)} \approx \frac{T_{mU}(s)}{T_{mU}(s)T_{mn}(s)} = \frac{1}{T_{mn}(s)}$$

On the other hand, for the frequencies beyond ω_c' where the conditions $|T_{mn}| \ll 1$ and $|T_{oU}T_{mn}| \ll 1$ are met, the loop gain becomes

$$T_{mL}(s) \approx T_{mU}(s)$$

Thus, the loading only alters the loop gain at frequencies below ω_c' and the crossover frequency and phase margin thus remain unchanged. The resulting loop gain was previously shown in Fig. **??** in Example **??**.

1.3.3 Section Summary

This section presented comprehensive loop gain analyses for load-coupled converters. The graphical analysis was adapted to yield a simple method to predict the asymptotic structure, crossover frequency, and phase margin of the converter loop gain. The outcomes of this analyses are summarized in Fig. 1.19 and Table 1.1.

The loading invariably affects the loop gain of all practical converters. The loading effects can be substantial in magnitude and wide in frequency. The loading could yield very involved loop gain characteristics, even crossing the 0 dB line three times. Even so, stability and performance of load-coupled converters can readily be determined from the minor loop gain, $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$.

1) The converter always remains stable as far as $T_{mn}(s)$ meets the Nyquist criterion, regardless of the extent and frequency range of the loading effect.

2) Very notably, the loop gain of the load-coupled converter is commonly given by the mirror image of the minor loop gain reflected by the 0 dB axis: $T_{mL}(s) \approx 1/T_{mn}(s)$. For this case, the crossover frequency and phase margin of the load-coupled converter are identical to those of the minor loop gain. When the minor loop gain has a sufficient phase margin and high crossover frequency, the load-coupled converter exhibits stability and good transient responses.

1.4 OUTPUT IMPEDANCE AND STEP LOAD RESPONSE ANALYSIS

In addition to the loop gain characteristics, the loading will influence other performance criteria of the converter. This section investigates the output impedance and step load response of load-coupled converters. First, the output impedance is studied based on the graphical analysis. Then, the transient response of the output voltage due to the step load change is predicted.

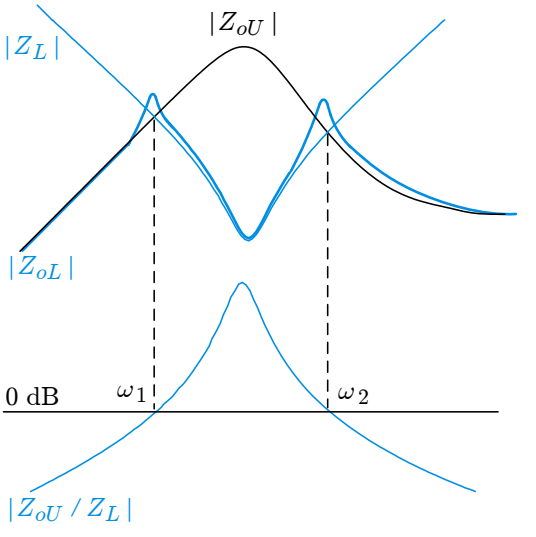


Figure 1.25 Construction of $|Z_{oL}|$ plot using $|Z_L|$, $|Z_{oU}|$, and minor loop gain.

1.4.1 Output Impedance Analysis

Referring to Table **??**, the output impedance of load-coupled converters, $Z_{oL}(s)$, is given by

$$\boxed{Z_{oL}(s) = Z_{oU}(s)\,\frac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}} \tag{1.20}$$

where $Z_{oU}(s)$ is the output impedance of the uncoupled converter and $Z_L(s)$ is the load impedance. The denominator of $Z_{oL}(s)$ contains the impedance ratio $Z_{oU}(s)/Z_L(s)$, which was defined as the minor loop gain $T_{mn}(s)$.

Simplification of (1.20) yields

$$Z_{oL}(s) \approx \begin{cases} \dfrac{Z_{oU}(s)}{\dfrac{Z_{oU}(s)}{Z_L(s)}} = Z_L(s) : \text{where } |Z_{oU}(s)/Z_L| \gg 1 \\[2ex] Z_{oU}(s) : \text{where } |Z_{oU}/Z_L| \ll 1 \end{cases} \tag{1.21}$$

Figure 1.25 shows the construction of the $|Z_{oL}|$ plot based on (1.21). The $|Z_{oL}|$ follows $|Z_{oU}|$ at low and high frequencies where $|Z_{oU}/Z_L| \ll 1$. On the other hand, $|Z_{oL}|$ tracks $|Z_L|$ in the frequency range of $\omega_1 < \omega < \omega_2$, where $|Z_{oU}/Z_L|$ rises

above the 0 dB line. The output impedance remains unaffected, $Z_{oL}(s) \approx Z_{oU}(s)$, if the condition $|Z_{oU}/Z_L| \ll 1$ is met for all frequencies.

The output impedance in Fig. 1.25 exhibits the two peaks around the 0 dB crossover frequencies of $T_{mn}(s)$, ω_1 and ω_2. The peak can be transformed into an underdamped second-order term in the s-domain expression, which arouses a decaying sinusoidal oscillation in the time-domain response. The output impedance will show an additional peaking if the phase margins of $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$ is not sufficiently large. Detailed analysis about the additional peaking will be provided in a later chapter.

Output Impedances of Load-Coupled Boost Converter **EXAMPLE 1.9**

This example illustrates the output impedances of the boost converter shown in Fig. 1.26(a). The parameters of the boost converter are slightly modified from those of the previous examples. Three load subsystems are considered with the different filter parameters.

- Load A: $L_f = 210\ \mu$H, $R_{lf} = 35\ \text{m}\Omega$, $C_f = 12500\ \mu$F, and $R_{cf} = 10\ \text{m}\Omega$
- Load B: $L_f = 5.25\ \mu$H, $R_{lf} = 15\ \text{m}\Omega$, $C_f = 4800\ \mu$F, and $R_{cf} = 10\ \text{m}\Omega$
- Load C: $L_f = 2.1\ \mu$H, $R_{lf} = 10\ \text{m}\Omega$, $C_f = 125\ \mu$F, and $R_{cf} = 35\ \text{m}\Omega$

The Bode plots of $|Z_{oU}|$ and three load impedances are shown in Fig. 1.26(b). Figure 1.26(c) displays the output impedance $|Z_{oL}|$ of the boost converter for the three different cases. For Load A and Load B, $|Z_{oL}|$ shows a peaking due to a small phase margin of the minor loop gain.

1.4.2 Step Load Response Analysis

This section deals with the transient response due to the step change in the load current. As demonstrated in Section 9.3.3, the transient behaviors of $v_O(t)$ can be inferred from the output impedance. Figure 1.27(a) depicts $|Z_{oU}|$ of the uncoupled converter and $|Z_{oL}|$ of the converter coupled with Load B. The general shape of $v_o(t)$ for the two converters are shown in Fig. 1.27(b).

In Section 9.3.3, the correlations between $Z_{oU}(s)$ and $v_O(t)$ for the uncoupled converter were discussed.

- The peak deviation in $v_O(t)$ is proportional to the product of the peak value of the output impedance $|Z_{oU}|_{peak}$ and size of the step load change I_{step}: $v_O(t)_{peak} \propto |Z_{oU}|_{peak} I_{step}$.

- The 5%-boundary settling time of $v_O(t)$ † is dictated by the first pole of $Z_{oU}(s)$, ω_p: $t_s = 3/\omega_p$.

†The time interval required for $v_O(t)$ to reach within 5% of the final value.

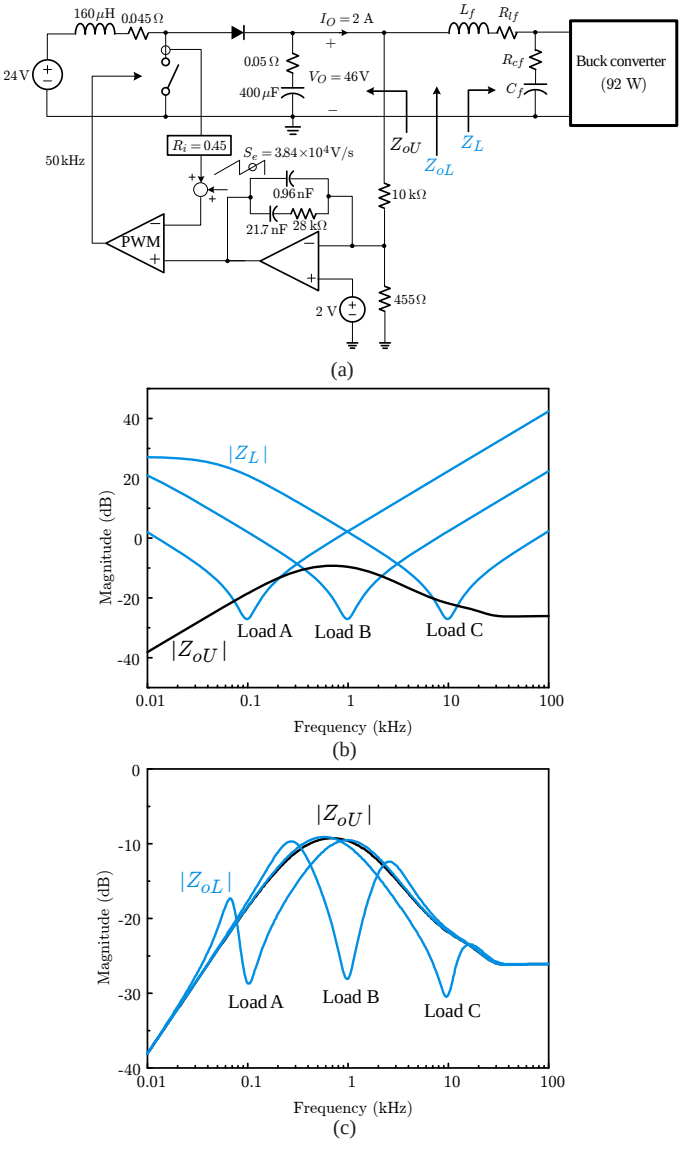


Figure 1.26 Output impedances of load-coupled boost converter. (a) Dc power conversion system. (b) Output impedance of uncoupled boost converter and load impedances. (c) Output impedances of load-coupled boost converter.

The behavior of $v_O(t)$ of the load-coupled converter is predicted from $|Z_{oL}|$. As previously discussed, the shape of $|Z_{oL}|$ signifies a decaying sinusoidal oscillation in $v_O(t)$.

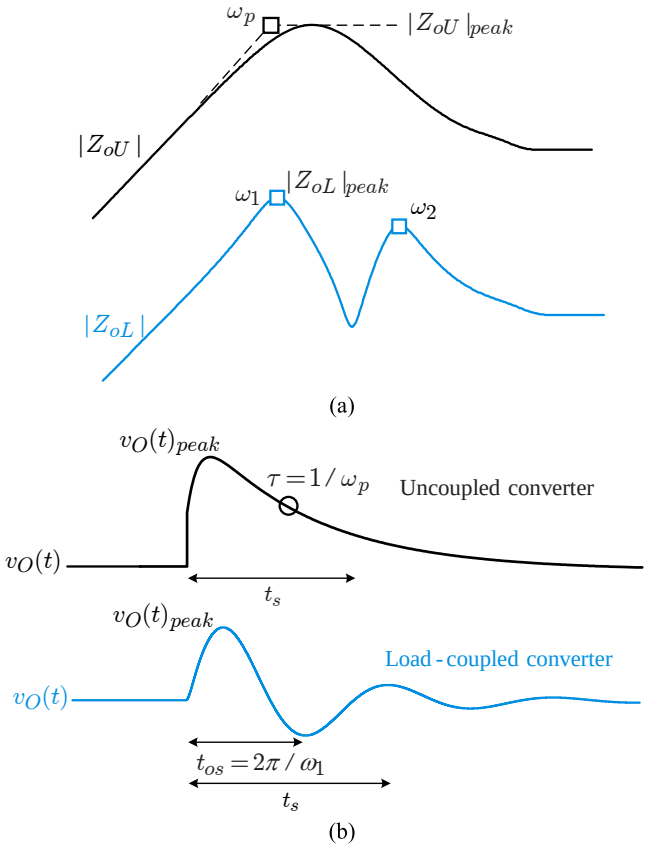


Figure 1.27 Output impedance and step load response. (a) Output impedances. (b) Step load responses.

- The peaks at ω_1 and ω_2 will both lead an oscillatory transient response. The frequency of the oscillation coincides with the frequency of the peak. Because $\omega_1 \ll \omega_2$, the high-frequency oscillation at ω_2 vanishes so fast that it will not show in $v_O(t)$ waveform. Thus, only the slow-decaying oscillation at ω_1 will appear in $v_O(t)$. The period of the decaying oscillation is given by $t_{os} = 2\pi/\omega_1$.

- The initial upsurge of the sinusoidal oscillation is proportionate to the product of the $|Z_{oL}|_{peak}$ at ω_1 and size of the step load change, I_{step}: $v_O(t)_{peak} \propto |Z_{oL}|_{peak} I_{step}$.

- The decaying rate of the sinusoidal oscillation will determine the settling time of $v_O(t)$. Based on the relationship between the frequency- and time-domain responses of a second-order system [3], the 5%-boundary settling time is estimated

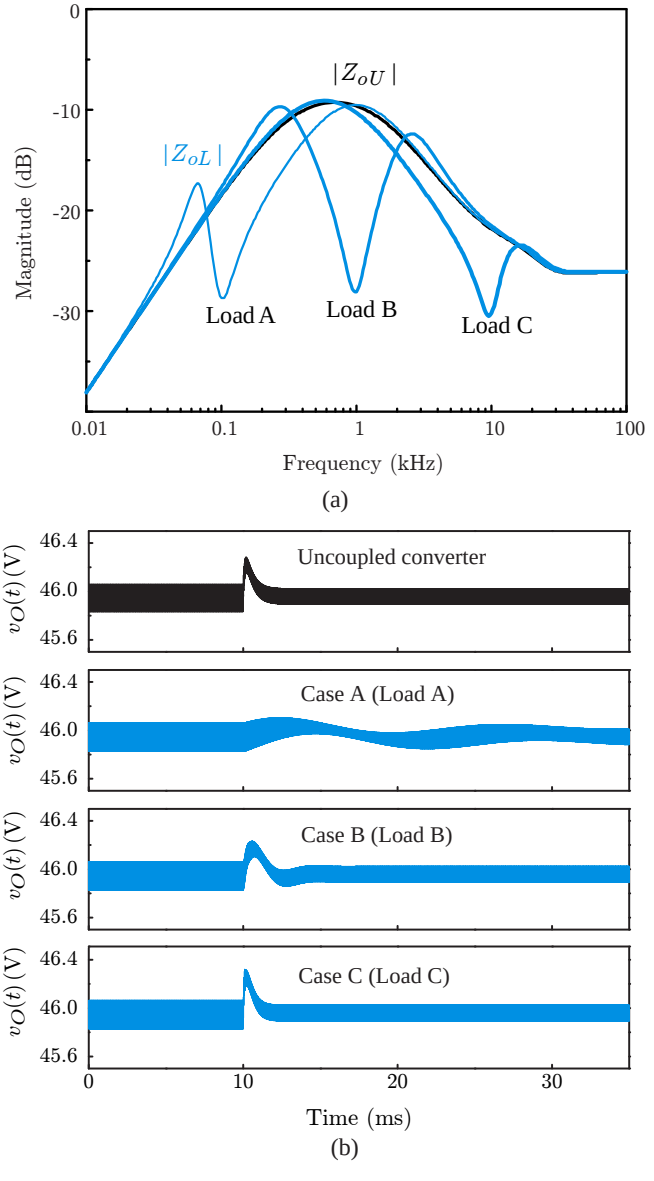


Figure 1.28 Output impedance and step load response. (a) Output impedances. (b) Step load responses.

as

$$t_s \approx 3 \left(\frac{100^\circ}{\mathrm{PM}_1} \right) \frac{1}{\omega_1} \tag{1.22}$$

where PM_1 is the phase margin of $T_{mn}(s)$ at ω_1.

Output Impedance and Step Load Response **EXAMPLE 1.10**

This example illustrates the output impedances and step load responses of the boost converter cited in Example 1.9. The output impedances of the boost converter are repeated in Fig. 1.28(a). The transient responses of the output voltage are shown in Fig. 1.28(b). The top waveform is $v_O(t)$ in response to a 2 A $\Rightarrow$ 1 A step decrease in the load current. The waveform reveals a good match to the prediction of Fig. 1.27.

The transient responses of $v_O(t)$ with the three different load subsystems are shown in the lower plots. Here, the equivalently same size of step load change was introduced in the load current of the downstream buck converter. For Case A and Case B, $v_o(t)$ shows an underdamped oscillation, as predicted in Fig. 1.27. For Case A, the oscillation is more persistent and sluggish due to a larger peaking at the lower frequency. Case B is the typical response that would occur most frequently in practical applications, as discussed in the previous section. The response of Case C is similar to that of the uncoupled converter because the output impedance largely remains the same except for high-frequency characteristics.

1.5 AUDIO-SUSCEPTIBILITY

This section covers the asymptotic analysis of the audio-susceptibility and input impedance of load-coupled converters. The audio-susceptibility is expressed as

$$A_{uL}(s) = A_{uU}(s)\,\frac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}} \tag{1.23}$$

where $A_{uU}(s)$ is the audio-susceptibility of the uncoupled converter and $Z_L(s)$ is the load impedance.

The expression in (1.23) is approximated as

$$A_{uL}(s) \approx \begin{cases} \dfrac{A_{uU}(s)}{\dfrac{Z_{oU}(s)}{Z_L(s)}} : \text{for frequencies where } |Z_{oU}/Z_L| \gg 1 \\ \\ A_{uU}(s) : \text{for frequencies where } |Z_{oU}/Z_L| \ll 1 \end{cases} \tag{1.24}$$

Figure 1.29 illustrates the construction of $|A_{uL}|$ based on (1.24). In the frequency range of $\omega_1 < \omega < \omega_2$, the minor loop gain $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$ is reflected as an additional attenuation in the audio-susceptibility of the load-coupled converter.

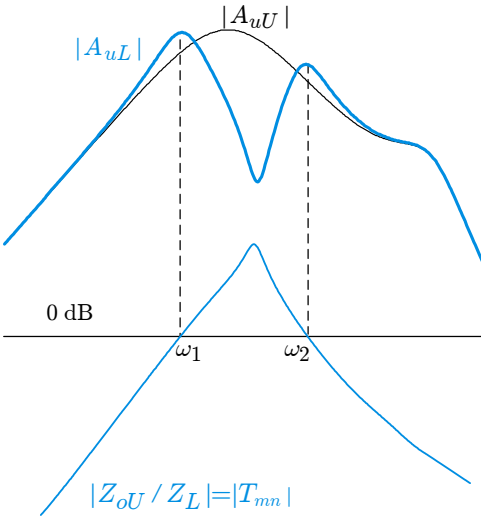


Figure 1.29 Construction of $|A_{uL}|$ plot using A_{uU} and minor loop gain.

The loading does not alter the audio-susceptibility provided that $|Z_{oU}/Z_L| \ll 1$ for all frequencies. The audio-susceptibility will show a peaking at the crossover frequencies of the minor loop gain, $T_{mn}(s) = Z_{oU}(s)/Z_L(s)$, if the phase margins are not sufficiently large.

EXAMPLE 1.11 Audio-Susceptibility of Load-Coupled Boost Converter

This example shows the audio-susceptibility of the boost converter used in Examples 1.9 and 1.10. Figure 1.30(a) shows the minor loop gains, while Fig. 1.30(b) illustrates the audio-susceptibilities of the load-coupled converter. The audio-susceptibility shows good agreement with the predictions of Fig. 1.29.

1.6 INPUT IMPEDANCE

Referring to Table **??**, the input impedance of the load-coupled converter is given by

$$Z_{iL}(s) = Z_{iU}(s)\,\frac{1 + \dfrac{Z_{oU}(s)}{Z_L(s)}}{1 + \dfrac{Z'_o(s)}{Z_L(s)}} \tag{1.25}$$

where $Z_{iU}(s)$ is the input impedance and $Z_{oU}(s)$ is the output impedance of the uncoupled converter. The impedance $Z'_o(s)$ represents the output impedance of the

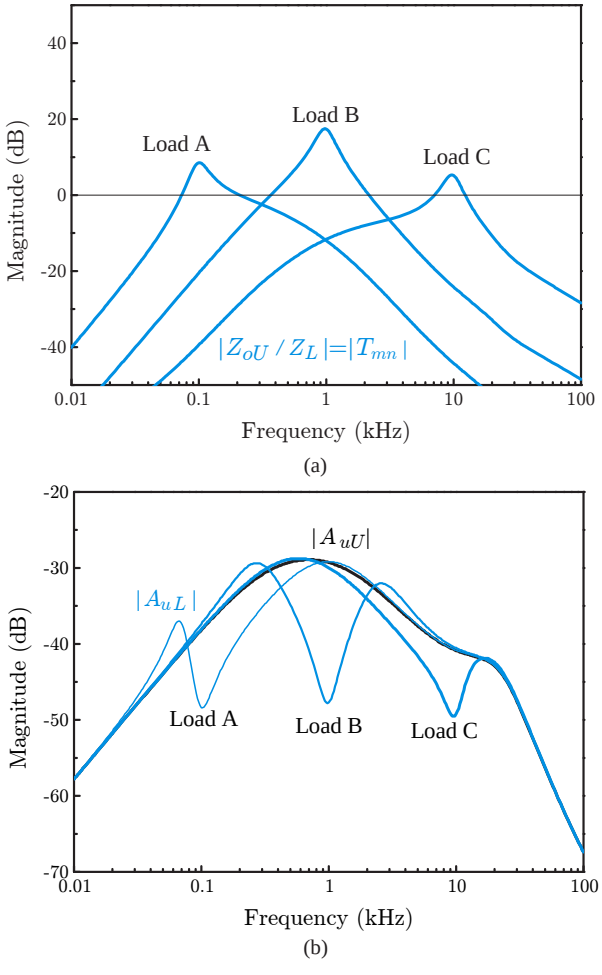


Figure 1.30 minor loop gain and audio-susceptibility. (a) minor loop gains. (b) Audio-susceptibilities.

uncoupled converter evaluated with the input port opened. For most converter cases, it can be shown that $|Z_L| \gg |Z_o'|$ so that $1 \gg |Z_o'/Z_L|$. This condition simplifies the $Z_{iL}(s)$ expression to

$$Z_{iL}(s) \approx Z_{iU}\left(1 + \frac{Z_{oU}(s)}{Z_L(s)}\right) \tag{1.26}$$

which can be further approximated to

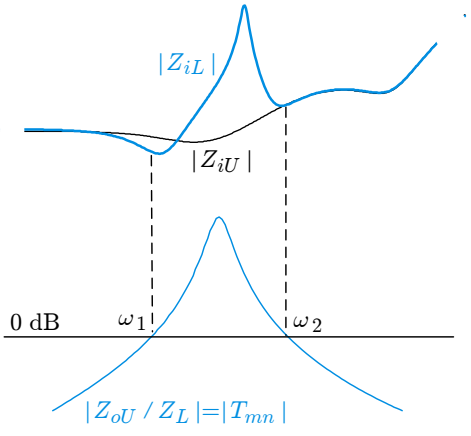


Figure 1.31 Construction of $|Z_{iL}|$ plot using $|Z_{iU}|$ and minor loop gain.

$$Z_{iL}(s) \approx \begin{cases} Z_{iU}(s)\dfrac{Z_{oU}(s)}{Z_L(s)} : \text{for frequencies where } |Z_{oU}/Z_L| \gg 1 \\ \\ Z_{iU}(s) : \text{for frequencies where } |Z_{oU}/Z_L| \ll 1 \end{cases} \tag{1.27}$$

Figure 1.31 illustrates the construction of $|Z_{iL}|$ based on (1.27). Here, the magnitude of the minor loop gain is projected as a magnitude boost in $|Z_{iL}|$.

EXAMPLE 1.12 Input Impedance of Load-Coupled Boost Converter

This example shows the input impedance of the boost converter employed in the previous dc power conversion system. Figure 1.32(a) shows the minor loop gains. Figure 1.32(b) illustrates the input impedance the load-coupled boost converter. The minor loop gain provides a magnitude boost for the input impedance in the frequencies where $|T_{mn}| = |Z_{oU}/Z_L| > 0$ dB.

1.7 CHAPTER SUMMARY

The impacts of the load subsystem are completely determined by the two specific impedances: the output impedance of the converter and the input impedance of the load subsystem, namely, the load impedance.

- The ratio of the converter output impedance to the load impedance, referred to as the minor loop gain $T_{mn}(s)$, governs the stability of the converter at the presence

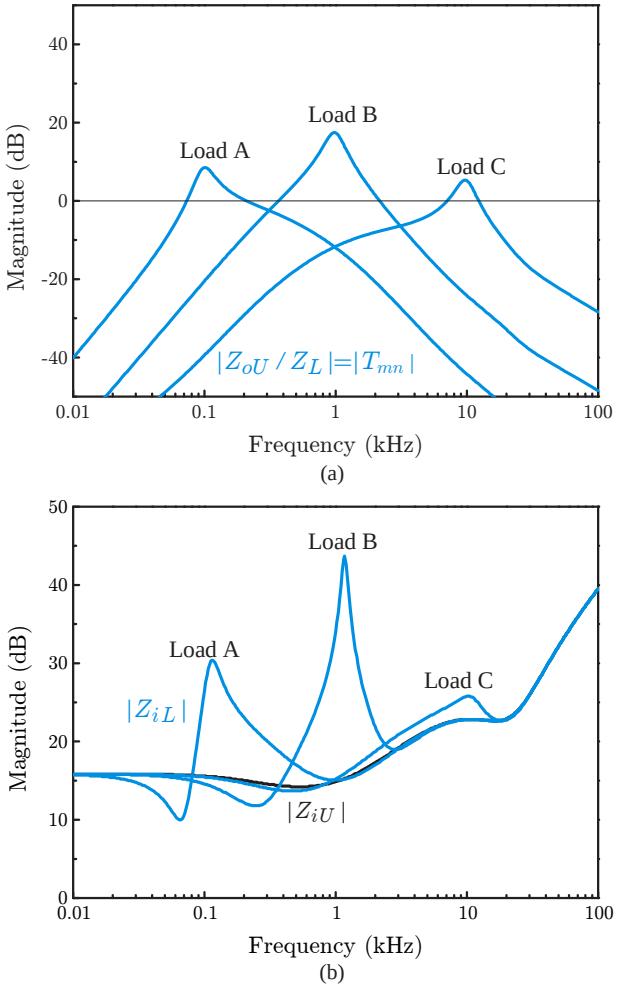


Figure 1.32 Minor loop gain and input impedances of load-coupled boost converter. (a) Minor loop gains. (b) Input impedances.

of the load subsystem. When the minor loop gain meets the Nyquist stability criterion, the load-coupled converter is stable. Otherwise, the converter becomes unstable after loading. The minor loop gain also dictates the performance of the converter loop gain. For wide frequency range, the converter loop gain is given by the inverse of the minor loop gain, $T_{mL}(s) \approx 1/T_{mn}(s)$, thereby yielding the same crossover frequency and phase margin as those of the minor loop gain. Thus, the minor loop gain determines both the absolute and relative stabilities of the converter.

- The ratio of the converter output impedance to the load impedance, or minor loop gain, reshapes the input impedance, loop gain, and output impedance of the converter, thereby utterly changing the small-signal dynamics. The overlap between the converter output impedance and load impedance is the key factor that determines the pattern and amount of the changes in the closed-loop performance. The impedance overlap is reflected as a dip in the audio-susceptibility and output impedance. On the other hand, the impedance overlap generates a boost in the input impedance. Nonetheless, these changes do not result in the performance degradation, provided that the load subsystem is properly designed.

  Load-coupled converters will become unstable only if the impedance overlap happens at low frequencies, where the load impedance behaves as a negative resistance. For this case, the minor loop gain violates the Nyquist stability criterion. However, the low-frequency impedance overlap hardly occurs in practice when converters and filter stages are properly designed.

Modern dc power conversion systems employ several cascaded stages of converters and filters, to achieve an efficient and reliable dc power distribution. The individual converters are designed and fabricated separately without any prior information about the system structure. When employed as a functional module in a dc power conversion system, the individual converter will be affected by the source and load subsystems, consisting of the other converters and filter stages in the system. An individual converter, termed as the uncoupled converter in this book, usually experiences substantial changes in the closed-loop performance and even crosses the borderline between stability and instability.

This chapter provided a comprehensive study on the stability and performance of the converter combined with the source and load subsystems in dc power conversion systems. The results of Middlebrook's EET, all established in Chapter 11, have been used to investigate the impacts of the load and source subsystems.

There are two main causes which adversely affect the dynamics of the converter combined with the source and load subsystems. The first cause is the constant power load whose input impedance behaves as a negative resistance at low frequencies. The converters themselves are the typical constant power load which can be the source of instability. The second cause is the resonance among the reactive circuit components in the converter and filter stages. The resonance produces a peaking/dipping in the output/input impedance of the source subsystem, converter, and load subsystem. The resonance intensifies the dynamic interaction between the source/load subsystem and the converter stage. For the worst case, the peaking or dipping triggers unstable oscillations when coupled with the negative input resistance of the converter stage. For all cases, the peaking or dipping increases the degree of the dynamic interaction. The escalated dynamic interaction generally makes the converter less stable and deteriorates the closed-loop performance. However, for some cases, the dynamic interaction does improve the stability and performance of the converter. As an example, the load subsystem can be designed to stabilize an unstable input filter-coupled converter, as demonstrated in Section 12.3.

Although the source subsystem and load subsystem both stimulate the dynamic interaction with the converter stage, the pattern and effects of the interactions are quite different. The characteristic features of the interactions from the load subsystem and the source subsystem are summarized below.

Load Subsystem Interaction The impacts of the load subsystem is completely determined by the two specific impedances: the output impedance of the converter and the input impedance of the load subsystem, namely, the load impedance.

- The ratio of the converter output impedance to the load impedance, referred to as the minor loop gain $T_{mn}(s)$, governs the stability of the converter at the presence of the load subsystem. When the minor loop gain meets the Nyquist stability criterion, the load-coupled converter is stable. Otherwise, the converter becomes unstable after loading. The minor loop gain also dictates the performance of the converter loop gain. For wide frequency range, the loop gain of the converter is given by the inverse of the minor loop gain, $T_{mL}(s) \approx 1/T_{mn}(s)$, thereby yielding the same crossover frequency and phase margin as those of the minor loop gain. Thus, the minor loop gain determines both the absolute and relative stabilities of the converter.

- The impedance ratio, or minor loop gain, reshapes the input impedance, loop gain, and output impedance of the converter, thereby utterly changing the small-signal dynamics. The overlap between the converter output impedance and load impedance is the key factor that determines the pattern and amount of the changes in the closed-loop performance. The impedance overlap is reflected as a dip in the audio-susceptibility and output impedance. On the other hand, the impedance overlap generates a boost in the input impedance. Nonetheless, these changes do not result in the performance degradation, provided that the load subsystem is properly designed.

  Load-coupled converters will become unstable only if the impedance overlap happens at low frequencies, where the load impedance behaves as a negative resistance, so that the equivalent loop violates the Nyquist stability criterion. However, the low-frequency impedance overlap hardly occurs in practice when converters and filter stages are properly designed.

Source Subsystem Interaction The impacts of the source subsystem can be assessed by investigating the output impedance of the source subsystem and the input impedances of the downstream converter. Here, the four different input impedances of the converter are needed to completely describe the impacts of the source subsystem. Thus, the source subsystem interaction is more complex than the load subsystem case.

- The stability of the source-coupled converter is determined by the peak magnitude of the output impedance of the source subsystem, $|Z_s|_{peak}$ and the low-frequency asymptote of the closed-loop input impedance of the converter, given

by $20\log V_S/I_S$. When $|Z_s|_{peak}$ falls below $20\log V_S/I_S$, the converter is stable. Otherwise, the converter becomes unstable.

- The impacts of the source subsystem on the other performance criteria are governed by the relative magnitudes of $Z_s(s)$ and the open-loop input impedances of the converter. The results of this analysis are summarized in Section 12.2.5, which covered the input filter interaction. The outcomes of the input filter interaction analysis can be directly extended to general load subsystems as far as the the output impedance of the source subsystem is available.

- The source subsystem interaction is less influential than the load subsystem interaction. Usually, the source subsystem partially modifies the closed-loop performance of the converter. For example, the source subsystem only adds a local dipping in the loop gain, leaving the crossover frequency and phase margin unchanged. This situation is quite different from the load subsystem case where the loop gain can be totally reshaped after loading.

This chapter provided detailed knowledge about the impacts of the load and source subsystems on the stability and performance of the converter stage. The results of this chapter can be used to analyze the dynamics of the converters employed in dc power conversion systems. More importantly, the results are very useful in designing and integrating the source and load subsystems for stable and efficient operation of the entire dc power conversion system.

It should be emphasized that the output impedance of the source subsystem and the input impedance of the load subsystem, which dictate the subsystem interactions and system stability, are mainly decided by the filter stages. Accordingly, the filter stage design is a critical element to secure the stability and performance of modern dc power conversion systems. The filter stage design, in consideration of the subsystem compatibility and system stability, will be covered in the next chapter.

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PROBLEMS

1.1** In Example 10.3 in Chapter 10, the modulator gain of the peak current mode control was derived from the expression

$$\bar{i}_L(t) = v_{con} - S_e dT_s - \frac{1}{2}(S_n + S_f)d(1-d)T_s$$

with the assumption that the slopes of the inductor current remain unchanged. Now, discard this assumption and introduce the perturbation to both S_n and S_f, in order to derive the feedforward gains from the input voltage/output voltage to duty ratio. Show that the feedforword gains are given by

Buck converter: $k_f = -\dfrac{D(1-D)T_s R_i}{2L}$ $\qquad k_r = 0$

Boost converter: $k_f = 0$ $\qquad k_r = -\dfrac{D(1-D)T_s R_i}{2L}$

Buck/boost converter: $k_f = -\dfrac{D(1-D)T_s R_i}{2L}$

$$k_r = -\frac{D(1-D)T_s R_i}{2L}$$

The above expressions differ from those of Ridley's model, but they coincide with the feedforward gains of Tan's model, as can be confirmed in Table 11.1.

1.2 Solve the expression (11.28)

$$\frac{\dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s}}{1+\dfrac{1}{R_i}\dfrac{1+\alpha}{sT_s}R_i H_e(s)} = \frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \quad \text{with} \quad \alpha = \frac{S_f - S_e}{S_n + S_e}$$

in order to derive the expression for $H_e(s)$ given in (11.19)

$$H_e(s) = \frac{sT_s}{e^{sT_s}-1}$$

1.3* Modify the procedures given in Example 11.5 to derive the expression for the feedforward gain from the output voltage, given in (11.46)

$$k_r' = \frac{(1-D)^2 T_s R_i}{2L}$$

1.4* The procedures for casting the control-to-output transfer function into the third-order expression

$$G_{vci}(s) = K_{vc}\frac{\left(1-\frac{s}{\omega_{rhp}}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_{pl}}\right)\left(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n^2}\right)}$$

are illustrated in Example 11.6.

a) Follow the procedures of Example 11.6 to derive the control-to-output transfer function of the boost converter given in Table 11.3

$$K_{vc} = \frac{D'R}{2R_i}\frac{1}{1+\frac{D'^3RT_s}{2L}(m_c-0.5)}$$

$$\omega_{pl} = \frac{2}{CR}+\frac{T_sD'^3}{LC}(m_c-0.5)$$

$$\omega_{rhp} = D'^2\frac{R}{L}$$

Specify the restrictions for the power stage parameters and operational conditions, which will improve the accuracy of the approximations.

b) Repeat **a)** for the buck/boost converter

$$K_{vc} = \frac{D'R}{(1+D)R_i}\frac{1}{1+\frac{D'^3RT_s}{(1+D)L}(m_c-0.5)}$$

$$\omega_{pl} = \frac{1+D}{CR}+\frac{T_sD'^3}{LC}(m_c-0.5)$$

$$\omega_{rhp} = \frac{D'^2}{D}\frac{R}{L}$$

1.5** Adaption of the new design procedures to a buck converter was illustrated in Example 11.8. Redesign the feedback controller for $Q_p = 0.4$, while keeping other design criteria unchanged. Compare the results of your design with those of Example 10.8.

1.6* Redesign the boost converter used in Example 11.9 with $Q_p = 0.32$, while keeping other design criteria the same. Compare the outcomes of your design with those of Example 10.16.

1.7* Example 11.11 proved the relationship

$$\frac{\omega_{ci}}{\omega_s} = \frac{Q_p}{2}$$

for the buck converter. Show that the above relationship also holds true for the boost and buck/boost converters.

1.8 Example 11.12 illustrated the relationship

$$K_{vc}\,\omega_{pl} \approx \frac{K_{vd}}{K_{id}R_i}\,\omega_{id}$$

for the buck converter. Verify that this relationship is also valid for the boost and buck/boost converters. Specify the conditions that enhance the accuracy of the approximation.

1.9* Figure P11.9 shows the off-line flyback converter with an optocoupler-isolated peak current mode control. The switching frequency of the converter is $\omega_s = 2\pi \cdot 65 \times 10^3$ rad/s. Perform the control design to meet the specifications of $Q_p = 0.8$ and $\omega_{cr} = 0.1\omega_{rhp}$, while adapting the other design guidelines practiced in Example 11.15. Specify values for $\{R_{sense}\ R_{com}\ C_{C1}\ R_D\ C_j\}$.

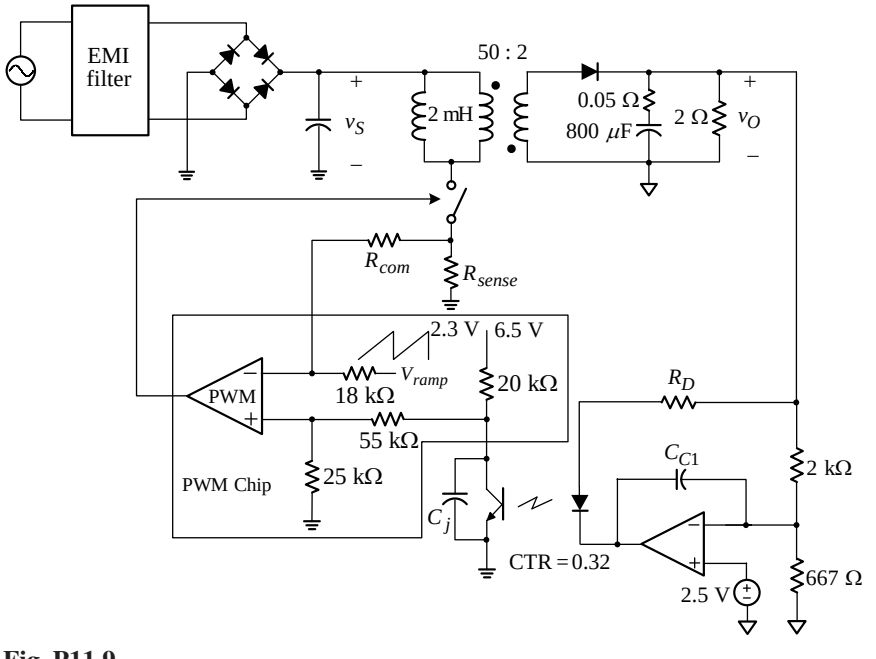

Fig. P11.9