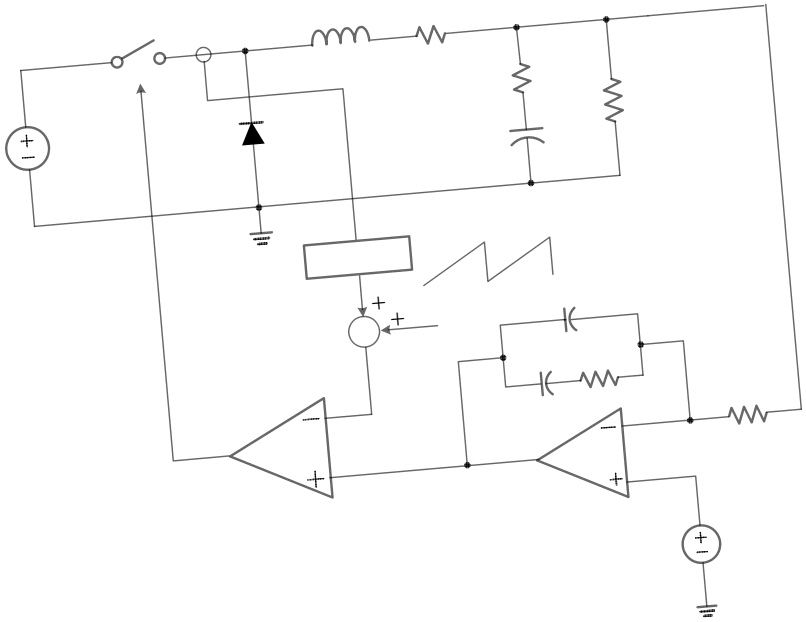
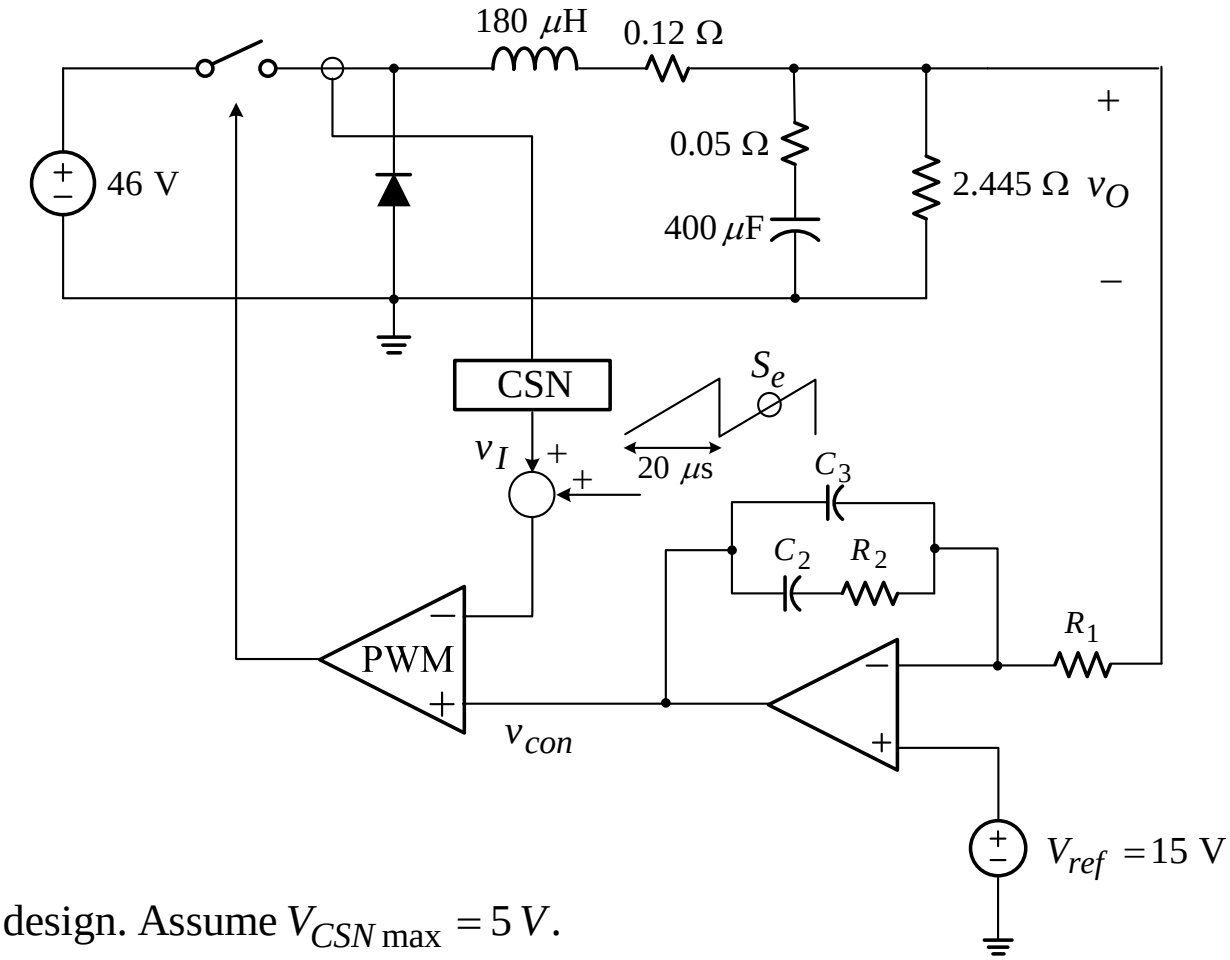
Final Term Project

Control Design and Performance Validation of Buck Converter



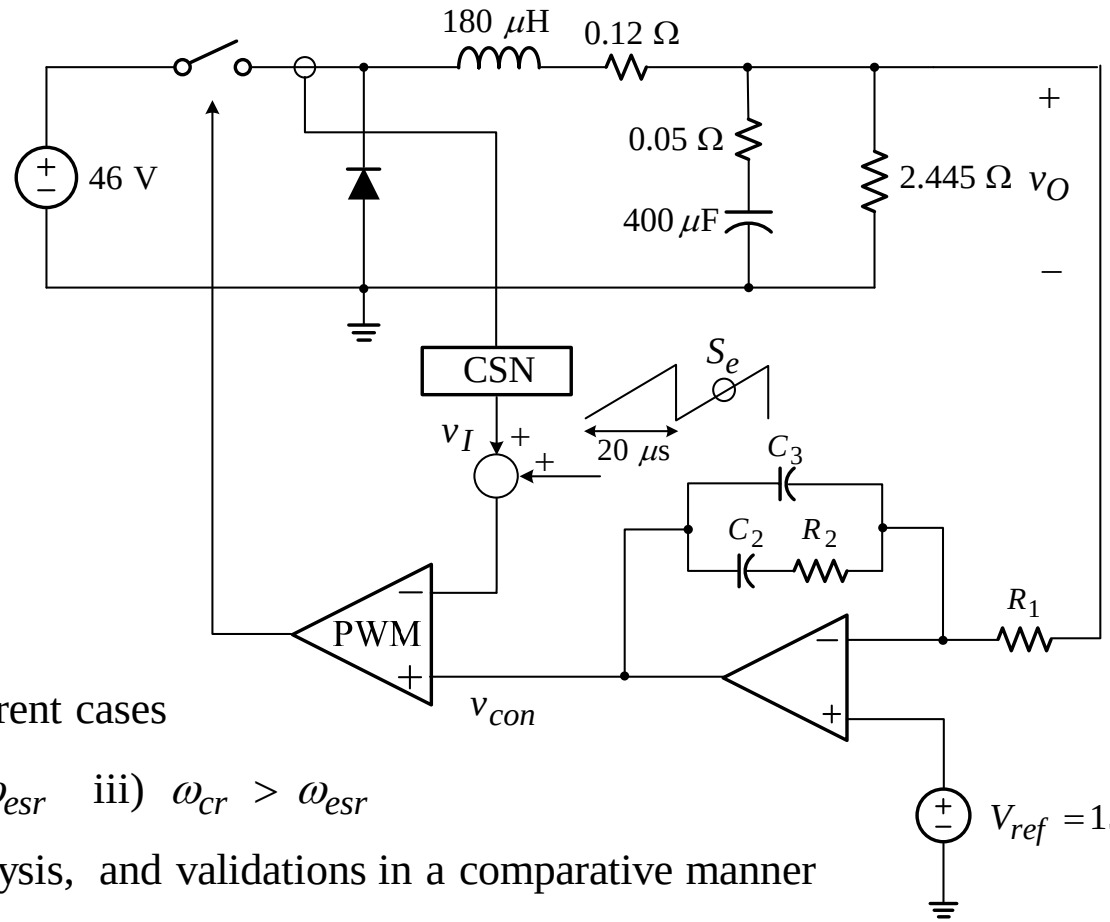
Buck Converter Design and Validation



1) Perform the current loop design. Assume $V_{CSN\,\max} = 5\,V$.

2) Analyze and validate $G_{vci}(s)$ of the converter.

Buck Converter Design and Validation



Consider the following three different cases

i) $\omega_{cr} < \omega_{esr}$ ii) $\omega_{cr} = \omega_{esr}$ iii) $\omega_{cr} > \omega_{esr}$

Perform the following design, analysis, and validations in a comparative manner

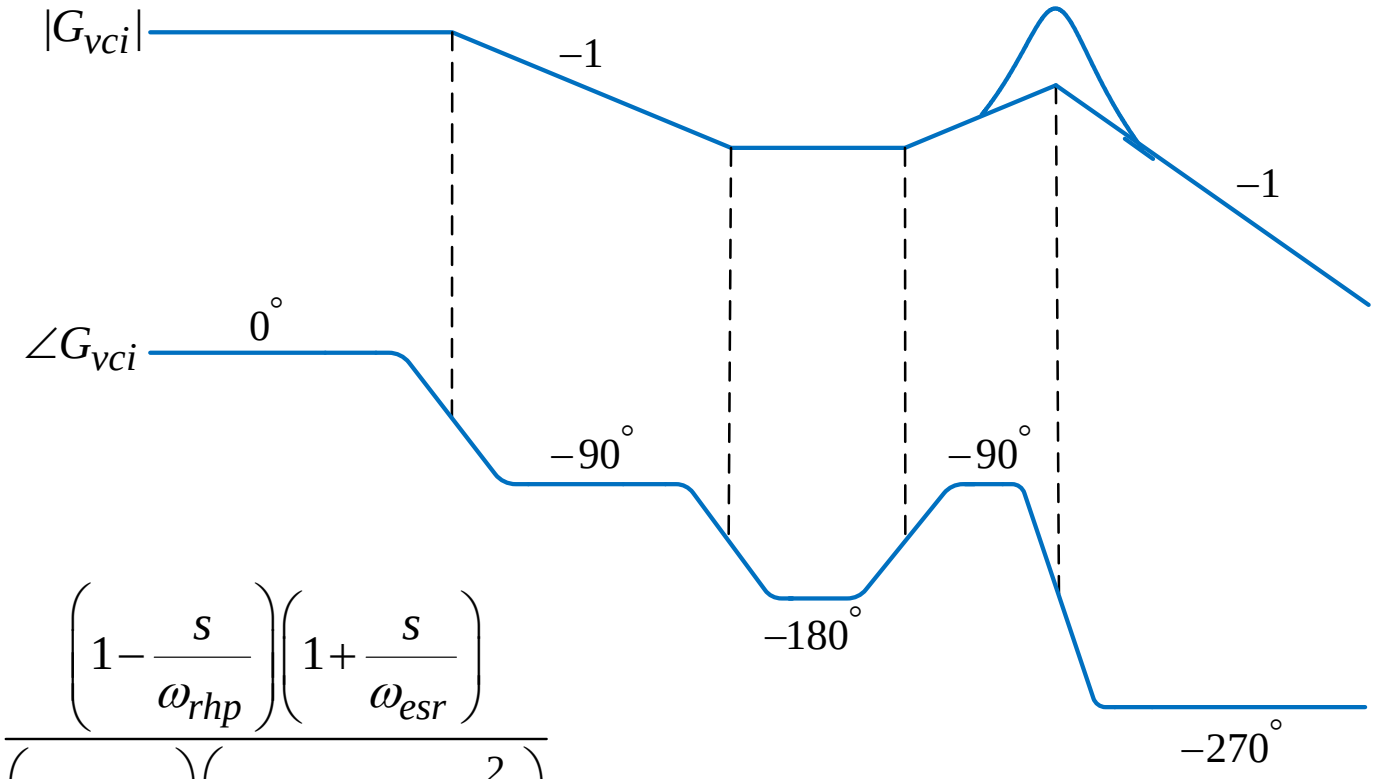
3) Perform the voltage loop design and validation.

4) Perform the loop gain analysis and validation.

5) Perform the output impedance analysis and validation.

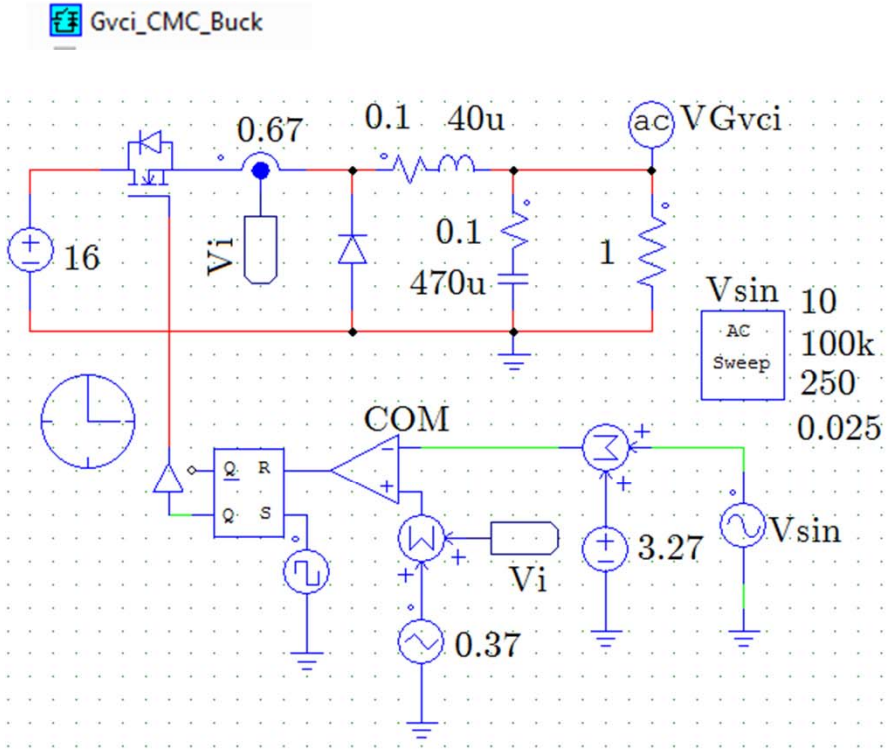
6) Perform the step load change response analysis and validation.

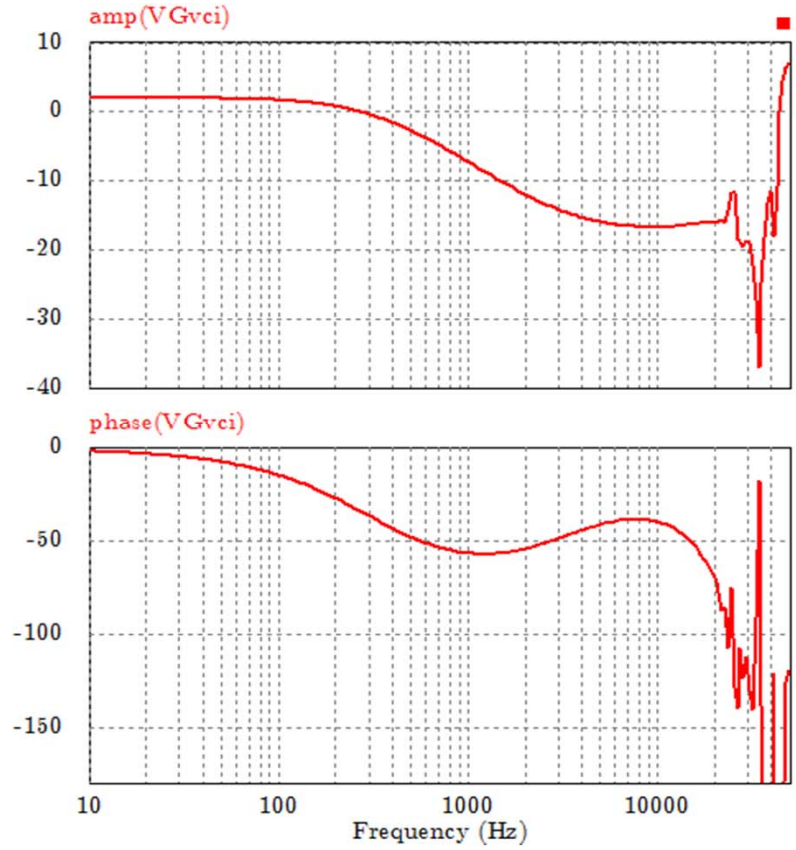
Asymptotic Plot of $G_{vci}(s)$



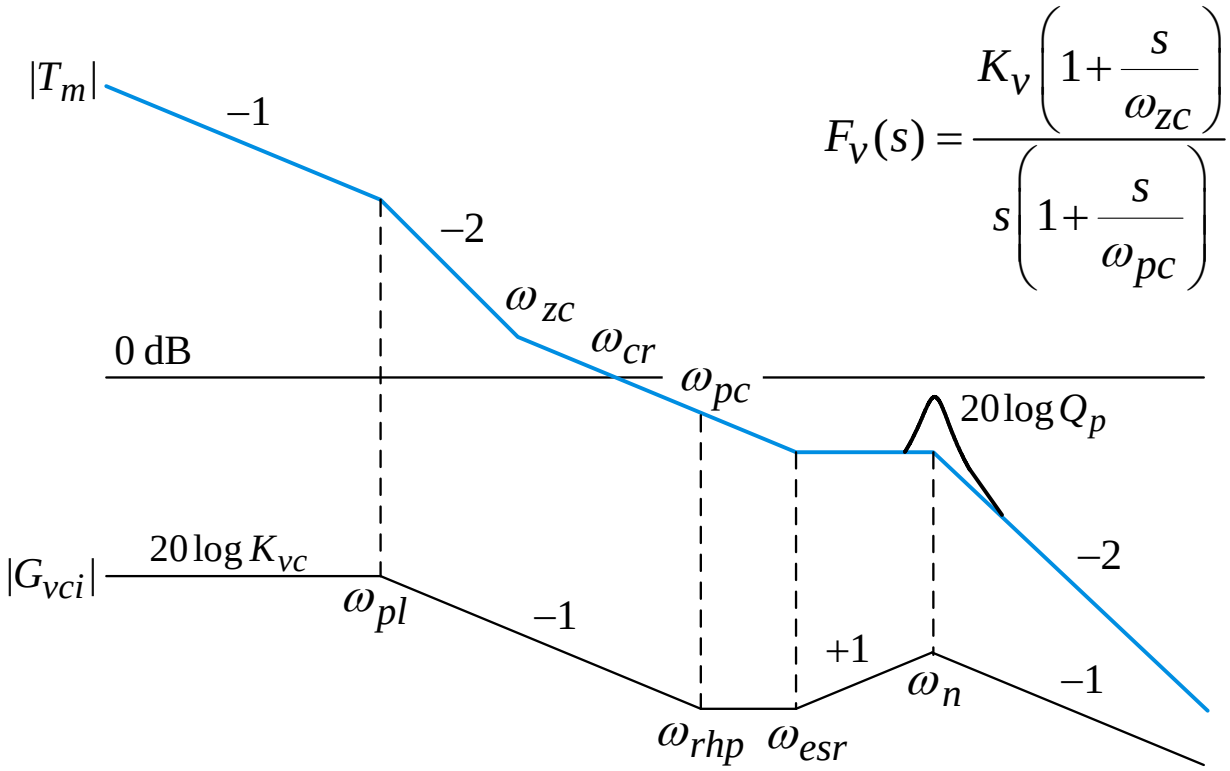
- $G_{vci}(s) \approx K_{vs} \dfrac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{\left(1+\dfrac{s}{\omega_{pl}}\right)\left(1+\dfrac{s}{Q_p\omega_n}+\dfrac{s^2}{\omega_n^2}\right)}$
- The double pole at half the switching frequency introduces a peaking of $20\log Q_p$.

$G_{vci}(s)$ Validation



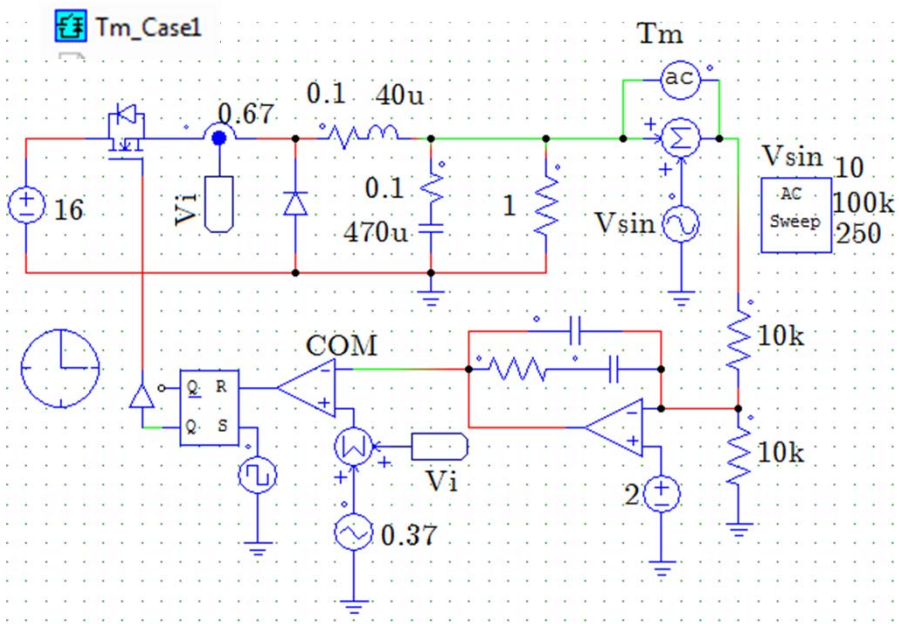


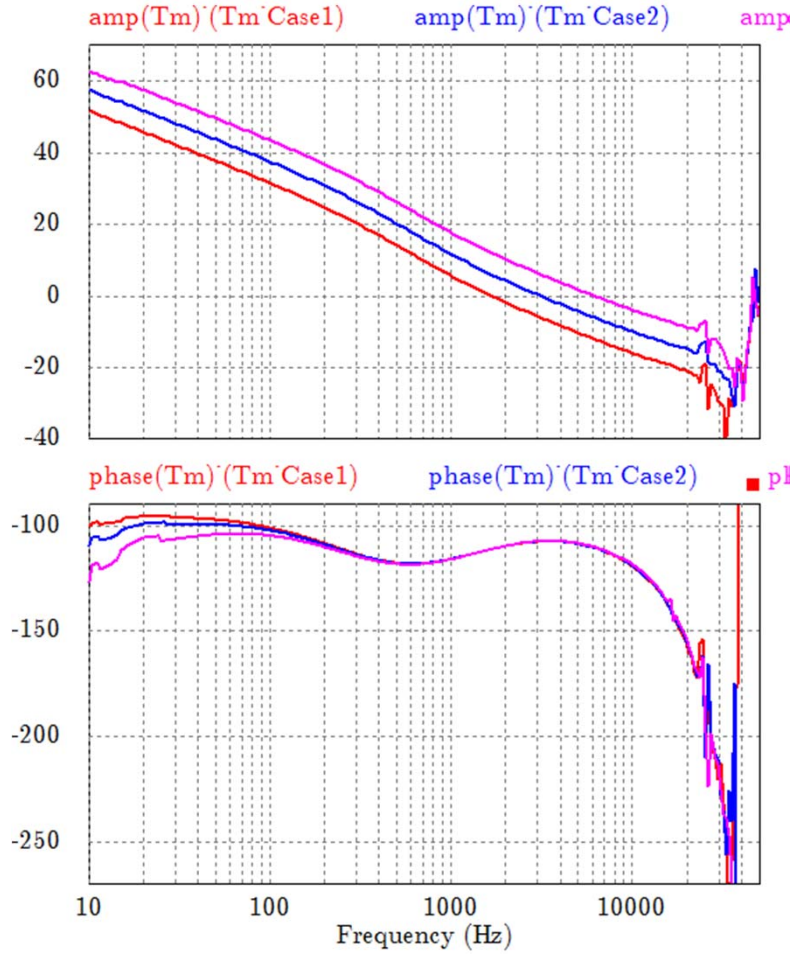
Loop Gain Asymptotic Plot



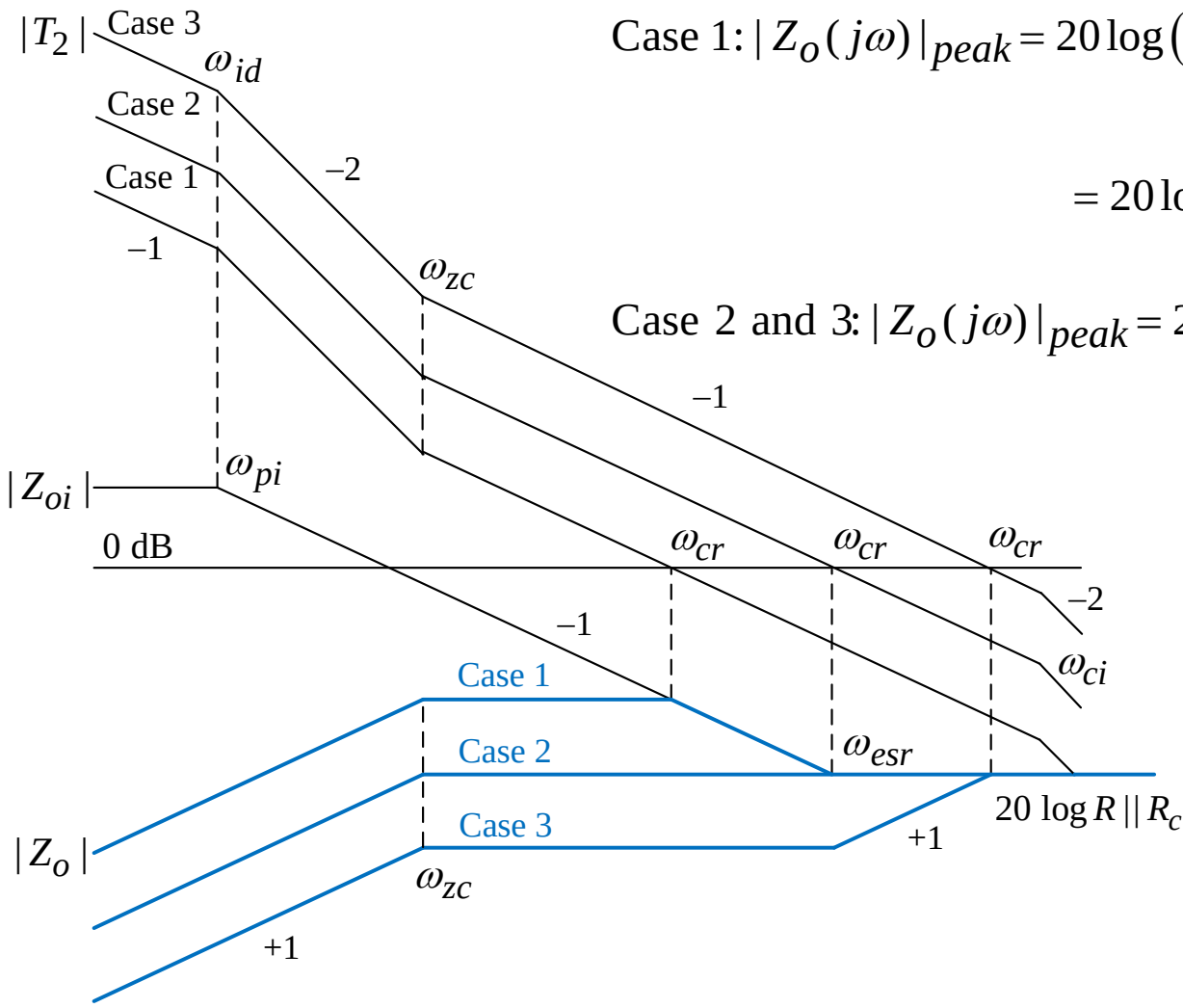
- $T_m(s) = G_{vci}(s)\,F_v(s) = K_{vc}\dfrac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{\left(1+\dfrac{s}{\omega_{pl}}\right)\left(1+\dfrac{s}{Q_p\omega_n}+\dfrac{s^2}{\omega_n^2}\right)}\dfrac{K_v\left(1+\dfrac{s}{\omega_{zc}}\right)}{s\left(1+\dfrac{s}{\omega_{pc}}\right)}$

Loop Gain Validation





Output Impedance Analysis



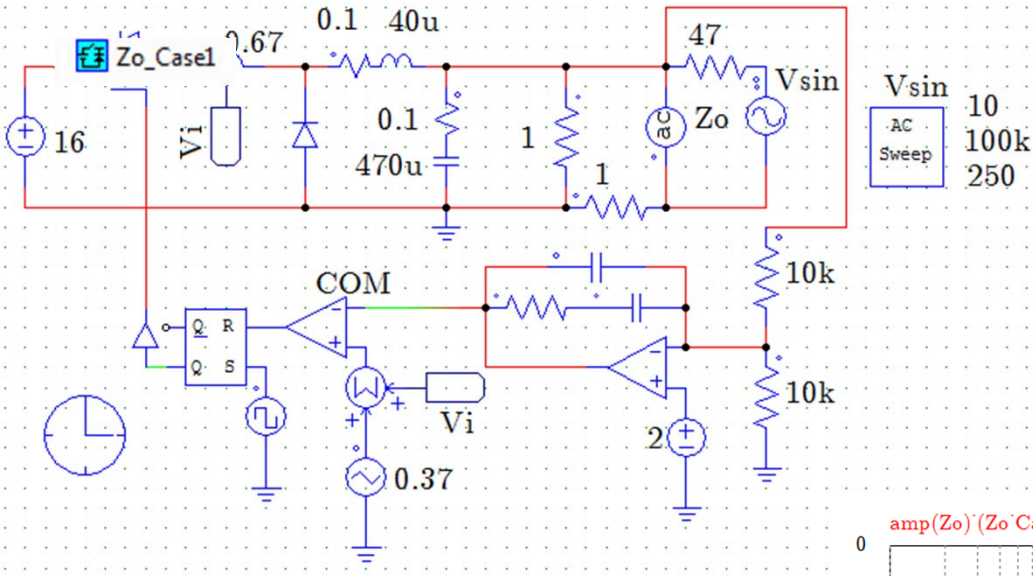
Case 1: $|Z_o(j\omega)|_{peak} = 20\log\left(R \,||\, R_c\right) + 20\log\left(\frac{\omega_{esr}}{\omega_{cr}}\right)$

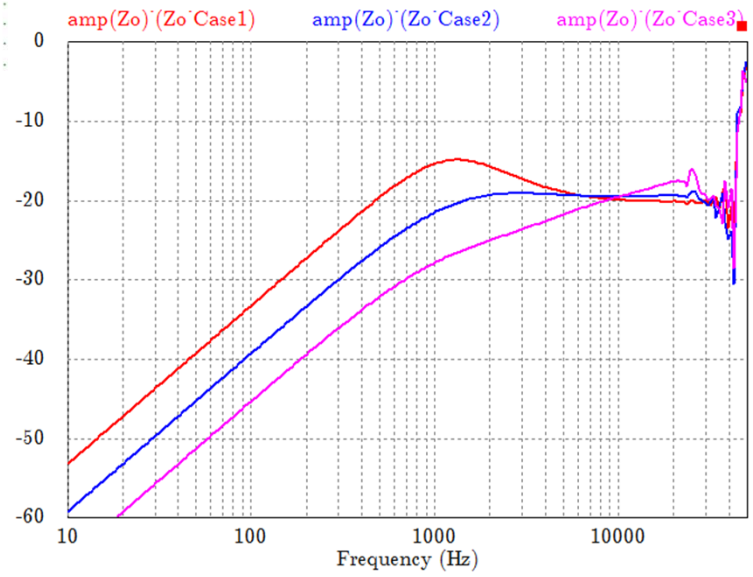
$= 20\log\left(R \,||\, R_c \frac{\omega_{esr}}{\omega_{cr}}\right)$

Case 2 and 3: $|Z_o(j\omega)|_{peak} = 20\log\left(R \,||\, R_c\right)$

Case 1: $\omega_{cr} < \omega_{esr}$ Case 2: $\omega_{cr} = \omega_{esr}$ Case 3: $\omega_{cr} > \omega_{esr}$

Output Impedance Validation





Step Load Response Validation