CHAPTER 1

UNCOUPLED CONVERTER AND EXTRA ELEMENT THEOREM

In the preceding chapters, we investigated the dynamics and control of standalone converters operating with an ideal voltage source and resistive load. We now turn our attention to the converters employed as a functional unit in generic dc power distribution systems.

A dc power distribution system has a complex structure. It consists of a number of cascaded/paralleled converters and filter stages. The operational environment of the individual converters in such systems is quite different from the case of standalone converters. Accordingly, we need new approaches to dealing with the converters in dc power distribution systems.

In this chapter, we establish appropriate methodologies for the control design and performance evaluation of the converters for dc power distribution applications. We will demonstrate that the control design is the same as the case of standalone converters with a resistive load. This rather surprising outcome leads to the following

straightforward statement. *The standard control design procedures developed earlier for resistive loads are still applicable to the converters for dc power conversion applications.*

On the other hand, the performance evaluation requires a new approach, because the converter dynamics in practical dc power distribution systems are too complex to be handled with conventional analysis techniques. We employ Middlebrook's extra element theorem (EET) as an instrumental tool for this study. This chapter presents general procedures for the dynamic analysis and performance evaluation based on the EET. Comprehensive analyses using the proposed procedures will be given in the next two chapters.

1.1 UNCOUPLED CONVERTER

This section introduces the idea of an uncoupled converter. Although simple in concept, the uncoupled converter greatly simplifies the design problem of the individual converters in dc power distribution systems.

1.1.1 Individual Converters in Dc Power Distribution Systems

Figure 1.1 depicts a common configuration of dc power distribution systems for data processors/computers. The system consists of a front-end converter, load converters, and intermediate filter stages. The front-end converter regulates the dc distribution bus through the voltage feedback compensation, $F_v(s)$. The load converters further change the dc bus voltage into other values.

A filter stage is employed at the input port of both the front-end converter and load converters. The input current of a PWM converter is either a pulsating waveform or a triangular waveform, containing a substantial amount of harmonic components. If the input current is directly drawn from the upstream side, large harmonic current components circulate in the system. The harmonic current components in turn produce excessive conducted electromagnetic interference (EMI), thereby failing to meet regulatory EMI standards. To avoid such a situation, a filter stage is placed at the input port of each individual converter converter. The filter stage locally bypasses the ac component of the input current so that only the smoothly-filtered dc current flows among the voltage source, front-end converter, and load converters.

In spite of the system complexity, all individual converters in Fig. 1.1 can be portrayed by one equivalent representation. Referring to the front-end converter, the formation of the equivalent representation is described as follows. The voltage source and filter stage before the front-end converter are considered as the source subsystem. Similarly, all the functional components after the front-end converter are collectively denoted as the load subsystem. The front-end converter receives the input voltage from the source subsystem and delivers a rated output current, i_O, to the load subsystem, while regulating the dc distribution bus.

Figure 1.2 shows the equivalent representation of the front-end converter. The source subsystem is represented by the Thevenin's form, consisting of an ideal voltage

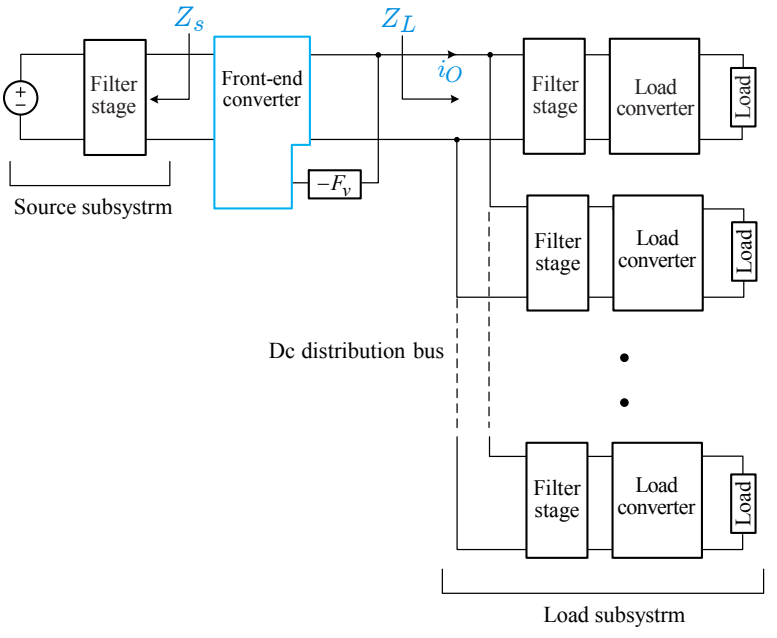


Figure 1.1 Dc power distribution system for data processors/computers.

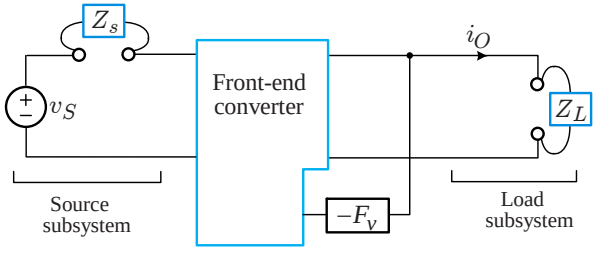


Figure 1.2 Equivalent representation of individual converter.

source, v_S, and series impedance, $Z_s(s)$. The $Z_s(s)$ is the source impedance seen by the front-end converter. On the other hand, the load subsystem is considered as a non-ideal current sink, which absorbs a rated current, while presenting certain load impedance $Z_L(s)$ to the front-end converter.

The equivalent representation can be used for the dynamic analysis and control design of the front-end converter. For this purpose, the parameters of the source and load subsystems should be identified. The source voltage v_S and the output current i_O are always predefined. However, the source impedance $Z_s(s)$ and load impedance $Z_L(s)$ are unknown or undefined until the actual source and load subsystems are

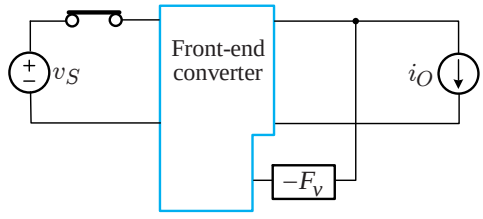


Figure 1.3 Uncoupled converter.

all fabricated and integrated with the front-end converter. Thus, the control design should be done without any knowledge about the source and load impedances.

1.1.2 Uncoupled Converter

To cope with the uncertainty in the source and load impedances, one can envisage a converter which is directly connected to an ideal dc source and loaded with an ideal current sink. The converter under such condition is shown in Fig. 1.3. The converter is termed as the *uncoupled converter* in the sense that the converter is decoupled from both the source subsystem and load subsystem in the small-signal point of view. The uncoupled converter can be designed as a standalone unit and tested using a dc source and current sink. In other words, we perform the design and verification of the converter in the absence of any knowledge about the source and load impedances.

Whenever the information about the source impedance and load impedance is available, we predict the converter performance in the real operation. This analysis will be done using Middlebrook's extra element theorem (EET). The EET allows us to evaluate the converter performance in the presence of $Z_s(s)$ and $Z_L(s)$, based on the predictions of the uncoupled converter and characteristics of $Z_s(s)$ and $Z_L(s)$ without analyzing the system all over again.

The converters in dc power distribution systems are treated as an uncoupled converter and designed independently from the unknown $Z_s(s)$ and $Z_L(s)$. When the characteristics of $Z_s(s)$ and $Z_L(s)$ are known, the converter performance will be evaluated based on Middlebrook's EET.

1.2 POWER STAGE DYNAMICS AND CONTROL DESIGN OF UNCOUPLED CONVERTER

We first investigate the power stage dynamics of uncoupled converters and later address the control design issue. The three basic converters with peak current mode control are considered. This section starts with the uncoupled buck converter.

1.2.1 Uncoupled Buck Converter

Figure 1.4 shows the circuit diagram and small-signal model of an uncoupled buck converter with current mode control. The converter is powered from an ideal voltage source and loaded with a current sink, as shown in Fig. 1.4(a). Referring to the small-signal model in Fig. 1.4(b), R_i is the gain of the current sensing network (CSN) and $F_v(s)$ represents the voltage feedback compensation. The expressions for the other gain blocks are given in Table **??**.

Discussions about the uncoupled buck converter are given in parallel with the case of the buck converter coupled with a resistive load. The converter with a resistive load is referred to as the *resistor-loaded converter*.

Power Stage Dynamics

Although the small-signal model of the uncoupled converter is largely the same as that of the resistor-loaded buck converter, there are some notable facets in Fig. 1.4(b). The ideal current sink presents an infinite load impedance, $Z_L(s) = \infty$. Therefore, the power stage is terminated with the filter capacitor in series with its esr. Yet, the output current I_O flowing into the current sink is incorporated into the power stage model as a resistive parameter

$$\boxed{R_{DC} = \frac{V_O}{I_O}} \tag{1.1}$$

where V_O is the output voltage and I_O is the output current delivered to the current sink. This resistive load parameter is termed as the *dc load parameter*, R_{DC}.

The average inductor current is determined as $I_L = I_O = V_O/R_{DC}$ for the buck converter. The dependent source in the PWM switch model, which was originally denoted as $I_L\hat{d}$ in the previous chapters, is now expressed as $(V_O/R_{DC})\hat{d}$. The current sink load renders the load impedance infinite, $Z_L(s) = \infty$, but it still affects the power stage dynamics through the dc load parameter, $R_{DC} = V_O/I_O$.

From the small-signal model with the condition $\hat{v}_s(s) = \hat{\imath}_o(s) = 0$, the duty ratio-to output transfer function is determined as

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd}\frac{1 + \dfrac{s}{\omega_{esr}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{1.2}$$

with

$$K_{vd} = V_S \tag{1.3}$$

$$\omega_{esr} = \frac{1}{CR_c} \tag{1.4}$$

$$\omega_o = \sqrt{\frac{1}{LC}} \tag{1.5}$$

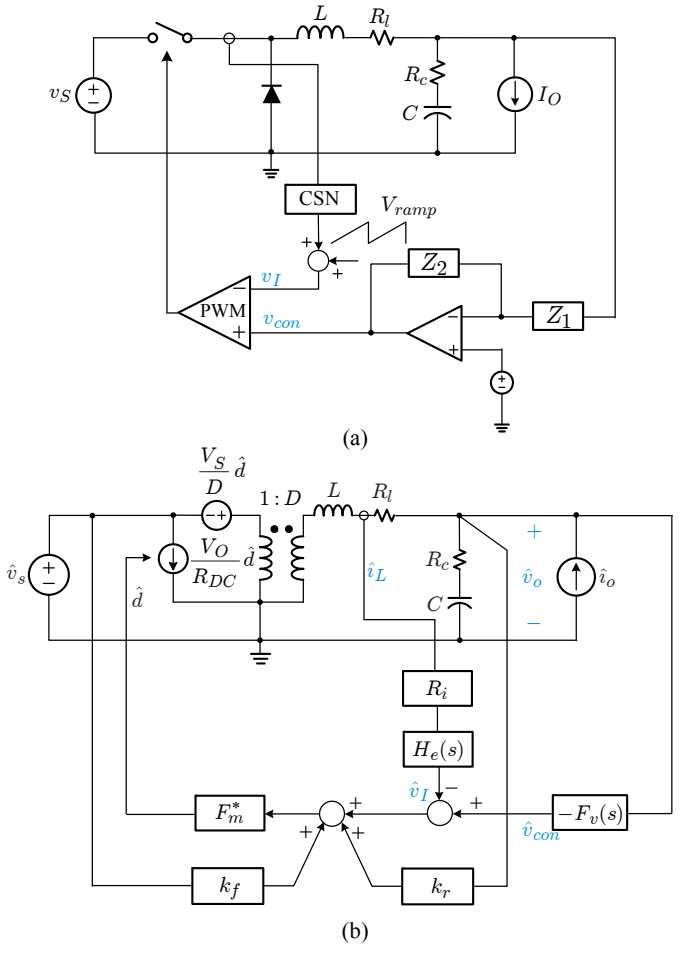


Figure 1.4 Uncoupled buck converter. (a) Circuit diagram. (b) Small-signal model.

and

$$Q = \frac{1}{R_l + R_c}\sqrt{\frac{C}{L}} \tag{1.6}$$

The duty ratio-to-inductor current transfer function is evaluated as

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = K_{id}\frac{s}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{1.7}$$

with

$$K_{id} = V_S C \tag{1.8}$$

When the transfer functions $G_{vd}(s)$ and $G_{id}(s)$ are assessed with the condition $\hat{v}_s(s) = 0$, the dependent current source $(V_O/R_{DC})\hat{d}$ is shorted and does not come into the power stage dynamics. Accordingly, the resistive load parameter R_{DC} does not appear in the $G_{vd}(s)$ and $G_{id}(s)$ expressions. This is the unique feature of the buck converter, which is not the case for the other converter topologies. For the boost and buck/boost converters, R_{DC} emerges as a key parameter in the $G_{vd}(s)$ and $G_{id}(s)$ expressions.

Control-to-Output Transfer Function with Current Loop Closed

Under the condition that the current loop is closed while the voltage loop is opened, the control-to-output transfer function is derived from Fig. 1.4(b)

$$G_{vci}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{con}(s)} = \frac{F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)}}{1 - k_r F_m^* \dfrac{\hat{v}_o(s)}{\hat{d}(s)} + R_i H_e(s) F_m^* \dfrac{\hat{i}_L(s)}{\hat{d}(s)}} \tag{1.9}$$

By following the procedures illustrated in Example **??**, the transfer function is casted into the following third-order approximation

$$G_{vci}(s) \approx K_{vc} \frac{1 + \dfrac{s}{\omega_{esr}}}{\left(1 + \dfrac{s}{\omega_{pl}}\right)\left(1 + \dfrac{s}{Q_p \omega_n} + \dfrac{s^2}{\omega_n^2}\right)} \tag{1.10}$$

with

$$\omega_{esr} = \frac{1}{CR_c} \tag{1.11}$$

$$Q_p = \frac{1}{\pi\left(\left(1 + \dfrac{S_e}{S_n}\right)D' - 0.5\right)} \tag{1.12}$$

and

$$\omega_n = \frac{\pi}{T_s} \tag{1.13}$$

The structure of the transfer function and the expressions for Q_p and ω_n are identical to those of Example **??** which dealt with a resistor-loaded buck converter. On the other hand, the expressions for K_{vc} and ω_{pl} are given by

$$K_{vc} = \frac{L}{R_i} \frac{1}{T_s(m_c D' - 0.5)} \tag{1.14}$$

and

$$\omega_{pl} = \frac{T_s(m_c D' - 0.5)}{LC} \tag{1.15}$$

with

$$m_c = 1 + \frac{S_e}{S_n} \tag{1.16}$$

where S_e is the slope of the compensation ramp and S_n is the slope of the sensed on-time inductor current.

Control Design

The power stage transfer functions of the uncoupled buck converter are different from those of the resistor-loaded buck converter. Nonetheless, as far as the control design is concerned, the uncoupled converter becomes the same as the resistor-loaded converter for the following reasons.

First, the criteria for the current loop design remain unchanged because the current loop always aims to properly damp the second-order term in the control-to-output transfer function. Second, the voltage loop design is based on the control-to-output transfer function $G_{vci}(s)$. Due to the same $G_{vci}(s)$ structure in the uncoupled and resistor-loaded converters, the two-pole one-zero compensation, originally used for the resistor-loaded converter,

$$F_v(s) = \frac{K_v\left(1 + \dfrac{s}{\omega_{zc}}\right)}{s\left(1 + \dfrac{s}{\omega_{pc}}\right)} \tag{1.17}$$

is also employed to the uncoupled buck converter. The guidelines for selecting the compensation pole, compensation zero, and integrator gain are unaltered. In particular, the integrator gain K_v is selected as

$$K_v = \frac{\omega_{zc}\,\omega_{cr}}{K_{vc}\,\omega_{pl}} \tag{1.18}$$

where ω_{zc} is the desired frequency of the compensation zero and ω_{cr} is the aimed loop gain crossover frequency. Because the selections of ω_{zc} and ω_{cr} are the same for the two converters, K_v will be identical if the product of K_{vc} and ω_{pl} remains invariant. For the uncoupled converter, it follows that

$$K_{vc}\omega_{pl} = \underbrace{\frac{L}{R_i}\frac{1}{T_s(m_cD' - 0.5)}}_{K_{vc}}\underbrace{\frac{T_s(m_cD' - 0.5)}{LC}}_{\omega_{pl}} = \frac{1}{R_iC} \tag{1.19}$$

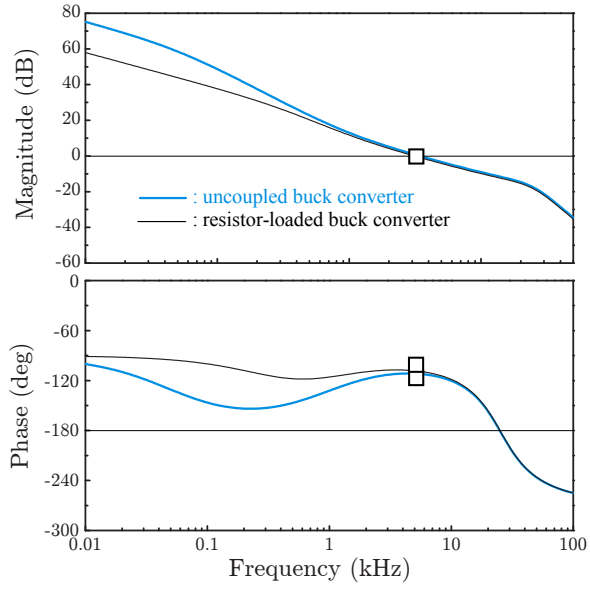


Figure 1.5 Loop gain characteristics of uncoupled and resistor-loaded converters

On the other hand, referring to Table **??**, the product of K_{vc} and ω_{pl} for the resistor-loaded converter is given by

$$\begin{aligned} K_{vc}\omega_{pl} &= \underbrace{\frac{R}{R_i}\frac{1}{1+\dfrac{RT_s}{L}(m_cD'-0.5)}}_{K_{vc}} \underbrace{\frac{1}{CR}\left(1+\frac{RT_s}{L}(m_cD'-0.5)\right)}_{\omega_{pl}} \\ &= \frac{1}{R_iC} \end{aligned} \tag{1.20}$$

The above analysis indicates that the voltage loop design for the uncoupled converter is the same as that of the resistor-loaded converter.

Now, the current loop and voltage loop designs proved to be identical for the uncoupled and resistor-loaded converters. Thus,the control design for uncoupled buck converters could adopt the standard design procedure intended for the resistor-loaded converters.

Performance of Uncoupled Buck Converter EXAMPLE 1.1

This example shows the utility of the preceding analysis using the current-mode controlled buck converter cited in Example 10.9. The converter regulates the output voltage at 4 Volts and loaded with a 1 Ω resistor. The original converter is referred to as the resistor-loaded converter. The uncoupled converter is formed by replacing the load resistor with a 4 Amps current sink, while using the same control design.

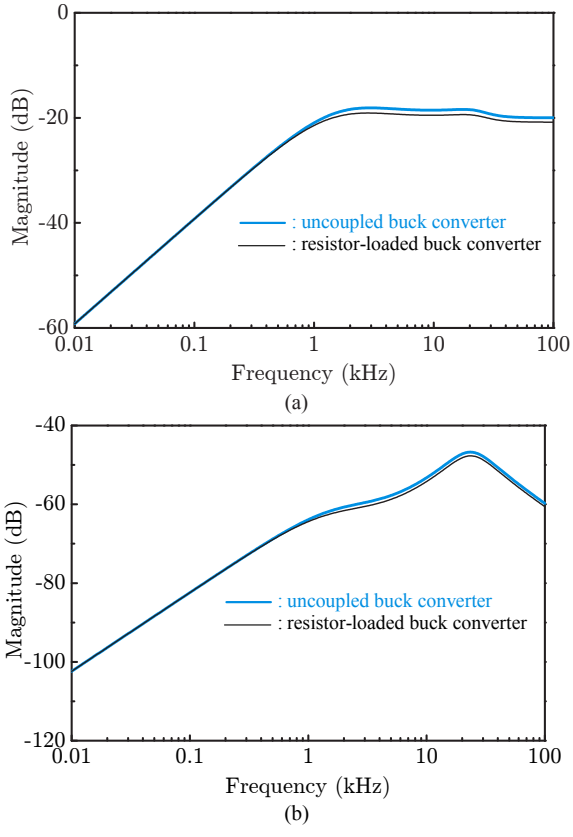


Figure 1.6 Output impedance and audio-susceptibility of uncoupled and resistor-loaded converters. (a) Output impedance. (b) Audio-susceptibility.

The loop gains of the two converters are shown in Fig. 1.5. While the two loop gains show some deviations at low frequencies, they have the same crossover frequency, phase margin, and gain margin. Figure 1.6 compares the output impedance and audio-susceptibility of the two converters. The transfer functions are almost identical.

Section Summary

The power stage dynamics of the uncoupled buck converter differ from those of the resistor-loaded buck converter. Nevertheless, the procedure and final result of the control design are the same in the two converters. Accordingly, the standard control design procedures, developed for resistive loads in the earlier chapters, are applicable to uncoupled buck converters without any modifications. As will be shown in later sections, this conclusion is also valid for all PWM converters with current mode

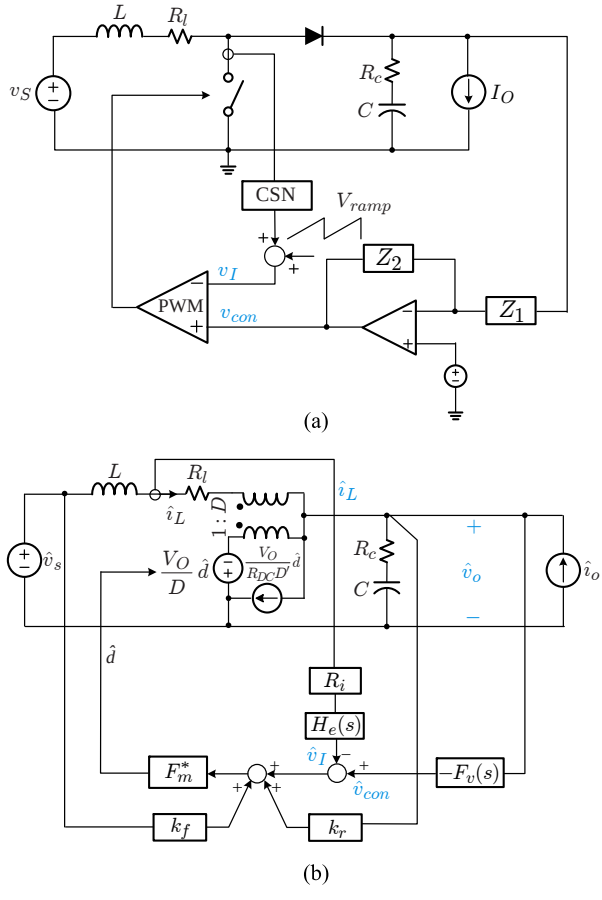


Figure 1.7 Uncoupled boost converter with peak current mode control. (a) Circuit diagram. (b) Small-signal model.

control or voltage mode control. The outcome of this section supports the validity and utility of the conventional control design which assumes that the converter is connected to a resistive load.

1.2.2 Uncoupled Boost Converter

This section deals with the uncoupled boost converter. Figure 1.7 shows the circuit diagram and small-signal model of the uncoupled boost converter employing peak current mode control. The expressions for the small-signal gain blocks in Fig. 1.7(b) are given in Table **??**.

The dependent current source in the PWM switch model is determined as

$$\boxed{I_L\hat{d} = \frac{I_O}{D'}\hat{d} = \frac{V_O}{R_{DC}D'}\hat{d}} \tag{1.21}$$

where $R_{DC} = V_O/I_O$ is the dc load parameter.

Power Stage Dynamics

From the small-signal model with the condition $\hat{v}_s(s) = \hat{i}_o(s) = 0$, the duty ratio-to output transfer function is evaluated as

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd}\frac{\left(1 - \dfrac{s}{\omega_{rhp}}\right)\left(1 + \dfrac{s}{\omega_{esr}}\right)}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{1.22}$$

with

$$K_{vd} = \frac{V_S\left(1 - \dfrac{R_l}{R_{DC}D'^2}\right)}{D'^2} \approx \frac{V_S}{D'^2} \tag{1.23}$$

$$\omega_{esr} = \frac{1}{CR_c} \tag{1.24}$$

$$\omega_{rhp} = \frac{R_{DC}D'^2 - R_l}{L} \approx \frac{R_{DC}D'^2}{L} \tag{1.25}$$

$$\omega_o = D'\sqrt{\frac{1}{LC}} \tag{1.26}$$

and

$$Q = \frac{D'}{R_l + R_cD'^2}\sqrt{\frac{C}{L}} \tag{1.27}$$

The duty ratio-to-inductor current transfer function is determined as

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = K_{id}\frac{1 + \dfrac{s}{\omega_{id}}}{1 + \dfrac{s}{Q\omega_o} + \dfrac{s^2}{\omega_o^2}} \tag{1.28}$$

with

$$K_{id} = \frac{V_S}{R_{DC}D'^3} \tag{1.29}$$

and

$$\omega_{id} = \frac{1}{C(R_{DC} + R_c)} \approx \frac{1}{CR_{DC}} \tag{1.30}$$

Unlike the case of the uncoupled buck converter where R_{DC} does not appear in the transfer functions, R_{DC} is a key parameter in the transfer functions of the uncoupled boost converter. In particular, R_{DC} determines the right-half plane (RHP) zero, ω_{rhp} in (1.25), in the duty ratio-to-output transfer function.

Control-to-Output Transfer Function with Current Loop Closed

The same as the uncoupled buck converter case, the control-to-output transfer function with the current loop closed is approximated into a third-order polynomial

$$G_{vci}(s) \approx K_{vc} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right)\left(1 + \frac{s}{Q_p\omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{1.31}$$

with

$$\omega_{rhp} = \frac{R_{DC}D'^2}{L} \tag{1.32}$$

$$K_{vc} = \frac{L}{R_i} \frac{1}{T_s D'^2(m_c - 0.5) + \frac{L}{R_{DC}D'}} \tag{1.33}$$

and

$$\omega_{pl} = \frac{T_s D'^2(m_c - 0.5) + \frac{L}{R_{DC}D'}}{\frac{LC}{D'}} \tag{1.34}$$

The other parameters of the transfer function are identical to those of the uncoupled buck converter.

Compensation Design

The control design of the uncoupled boost converter is the same as the case of the resistor-loaded boost converter.

1) For both the uncoupled and resistor-loaded boost converters, the integrator gain of the voltage feedback compensation is chosen as

$$K_v = \frac{\omega_{zc}\omega_{cr}}{K_{vc}\omega_{pl}} \tag{1.35}$$

2) For the uncoupled converter, the product of K_{vc} and ω_{pl} is given by

$$K_{vc}\omega_{pl} = \frac{D'}{CR_i} \tag{1.36}$$

from (1.33) and (1.34).

3) Referring to Table **??**, K_{vc} and ω_{pl} for the resistor-loaded converter are given by

$$K_{vc} = \frac{L}{R_i} \frac{1}{T_s D'^2(m_c - 0.5) + \frac{2L}{RD'}} \tag{1.37}$$

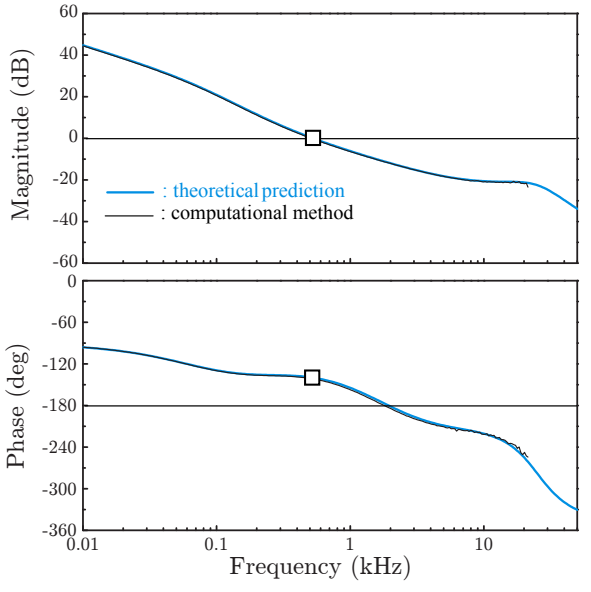


Figure 1.8 Loop gain characteristics of uncoupled boost converter.

and

$$\omega_{pl} = \frac{T_s D'^2 (m_c - 0.5) + \dfrac{2L}{RD'}}{\dfrac{LC}{D'}} \tag{1.38}$$

This indicates the product of K_{vc} and ω_{pl} for the resistor-loaded converter is also given by (1.36). Thus, the control design for the two converter cases is identical.

EXAMPLE 1.2 Performance of Uncoupled Boost Converter

Figures 1.8 and 1.9 show the performance of the uncoupled boost converter. The boost converter in Example **??** is revisited in this example. The same operational conditions and circuit parameters are employed, but the converter is loaded with an ideal current sink.

The loop gain is displayed in Fig. 1.8. The loop gain crosses the 0 dB line at $\omega_c = 2\pi \cdot 400$ rad/s with a phase margin of 55°. Figure 1.9 shows the output impedance of the uncoupled boost converter. The output impedance shows a peaking around the crossover frequency of the loop gain. At high frequencies, the output impedance settles at the high-frequency asymptote of $20 \log R_c = 20 \log 0.05 = -26$ dB.

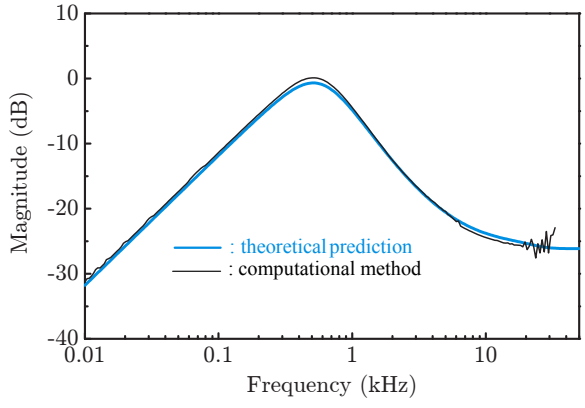


Figure 1.9 Output impedance uncoupled boost converter.

1.2.3 Uncoupled Buck/Boost Converter

The results of the previous two sections are be extended to the uncoupled buck/boost converter operating with peak current mode control.

The duty ratio-to output transfer function of the uncoupled buck/boost converter is given by

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = K_{vd} \frac{\left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{esr}}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{1.39}$$

with

$$K_{vd} = \frac{V_S\left(1 - \frac{R_l D}{R_{DC} D'^2}\right)}{D'^2} \approx \frac{V_S}{D'^2} \tag{1.40}$$

$$\omega_{esr} = \frac{1}{CR_c} \tag{1.41}$$

$$\omega_{rhp} = \frac{R_{DC} D'^2 - R_l D}{DL} \approx \frac{R_{DC} D'^2}{DL} \tag{1.42}$$

$$\omega_o = D'\sqrt{\frac{1}{LC}} \tag{1.43}$$

and

$$Q = \frac{D'}{R_l + R_c D'^2}\sqrt{\frac{C}{L}} \tag{1.44}$$

The duty ratio-to-inductor current transfer function is evaluated as

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = K_{id}\frac{1+\dfrac{s}{\omega_{id}}}{1+\dfrac{s}{Q\omega_o}+\dfrac{s^2}{\omega_o^2}} \tag{1.45}$$

with

$$K_{id} = \frac{DV_S}{R_{DC}D'^3} \tag{1.46}$$

and

$$\omega_{id} = \frac{D}{C(R_{DC}+R_c)} \approx \frac{D}{CR_{DC}} \tag{1.47}$$

The control-to-output transfer function with the current loop closed is determined as

$$G_{vci}(s) \approx K_{vc}\frac{\left(1-\dfrac{s}{\omega_{rhp}}\right)\left(1+\dfrac{s}{\omega_{esr}}\right)}{\left(1+\dfrac{s}{\omega_{pl}}\right)\left(1+\dfrac{s}{Q_p\omega_n}+\dfrac{s^2}{\omega_n^2}\right)} \tag{1.48}$$

with

$$\omega_{rhp} = \frac{R_{DC}D'^2}{DL} \tag{1.49}$$

$$K_{vc} = \frac{L}{R_i}\frac{1}{T_sD'^2(m_c-0.5)+\dfrac{DL}{R_{DC}D'}} \tag{1.50}$$

and

$$\omega_{pl} = \frac{T_sD'^2(m_c-0.5)+\dfrac{DL}{R_{DC}D'}}{\dfrac{LC}{D'}} \tag{1.51}$$

The product of the parameters K_{vc} and ω_{pl} is given by

$$K_{vc}\omega_{pl} = \frac{D'}{CR_i} \tag{1.52}$$

As is the case of the buck and boost converters, (1.52) is equally valid to the resistor-loaded converter. Therefore, the control design for an uncoupled buck/boost converter is the same as that of the resistor-loaded converter. Furthermore, this conclusion is extended to the converters loaded with an arbitrary load impedance.

1.3 COUPLED CONVERTERS AND MIDDLEBROOK'S EXTRA ELEMENT THEOREM

The previous section covered the dynamic analysis and control design of uncoupled converters. An uncoupled converter was treated as a standalone functional unit. However, in real dc power conversion applications, converters always operate together with the source subsystem and load subsystem. The coupled converter with the source and load subsystems is referred to as a *coupled converter*.

The performance of a coupled converter is usually affected by the load and source impedances. The objective of this section is to develop an analytic method for investigating the performance of coupled converters. We assume that an uncoupled converter is properly designed and its performance is validated. We further postulate that the impedance characteristics of the source and load subsystems are now available. Based on these assumptions, we will establish a systematic approach to predicting the performance of the converter coupled with the source and load subsystems.

An ideal instrumental tool for the dynamic analysis of coupled converters is the *extra element theorem* (EET). The EET shows how a transfer function is altered by the addition of an *extra element* to the original system. In other words, *the theorem allows one to determine the effects of the extra element on any transfer function of interest, without solving the system all over again*. For example, the loop gain of the converter combined with an actual load subsystem can be determined from the loop gain of the uncoupled converter and the impedance characteristics of the load subsystem – the load impedance.

This section first presents the EET in its simplest form along with its proof. Second, the EET is applied to the converter combined with a load subsystem, resulting in the equations for the converter performance in the presence of the load impedance. The EET is then adapted to the converter coupled with a non-ideal voltage source. The results show the impacts of the source impedance on the converter performance. Lastly, this section discusses how to use the EET to evaluate the performance of converters coupled with an actual source subsystem and also connected to a real load subsystem.

The aim of this section is to present the analytical basis for the performance evaluation of coupled converters. Comprehensive dynamic analyses using the proposed method will be separately treated in the next two chapters.

1.3.1 Middlebrook's Extra Element Theorem

This section briefly describes the expression, proof, and examples of the EET. The EET was originally introduced in [1] and [2] by R. D. Middlebrook. In a later reference [3], V. Vorpérion documented the theorem in a textbook format, along with numerous examples. Some applications of the EET to the PWM converter analysis were reported in [4]-[8].

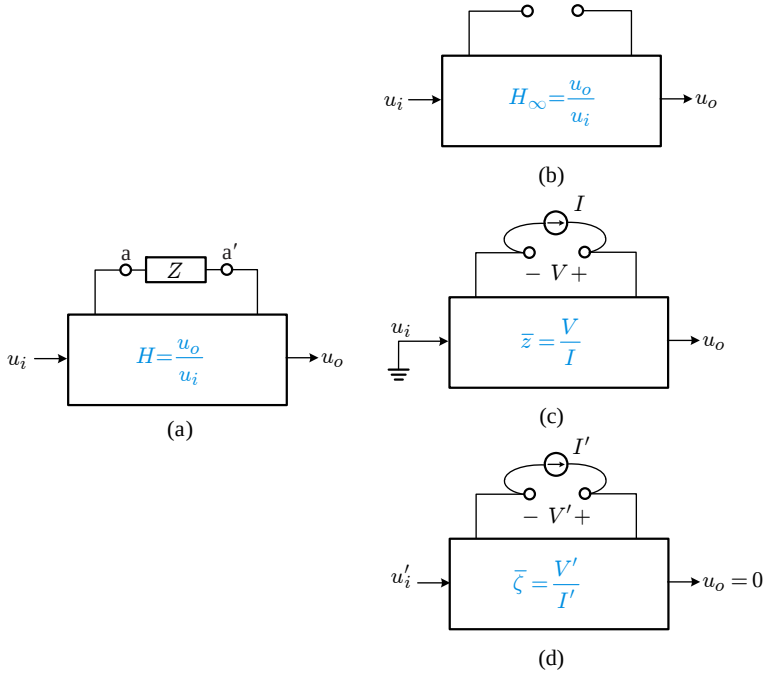


Figure 1.10 Pictorial illustration of extra element theorem. (a) Transfer function of interest. (b) Open-circuit transfer gain. (c) Driving point impedance. (d) Null driving point impedance.

Extra Element Theorem

The extra element theorem (EET) states that any transfer gain of an arbitrary network can be expressed as a bilinear function of the impedance of any one of its components. Figure 1.10 is a pictorial illustration of the EET. The transfer gain $H(s)$ of a linear network is defined in Fig. 1.10(a). The EET expresses the transfer gain $H(s)$ as

$$H(s) = \frac{u_o(s)}{u_i(s)} = H_\infty(s)\frac{1+\dfrac{\bar{\zeta}(s)}{Z(s)}}{1+\dfrac{\bar{z}(s)}{Z(s)}} \tag{1.53}$$

where $u_i(s)$ is the input variable, $u_o(s)$ is the output variable, and $Z(s)$ represents the impedance of the specific circuit component that exists across the $a-a'$ branch and is designated as the *extra element*. The other transfer functions in the expression (1.53) are described below and illustrated in Figs. 1.10(b) through 1.10(d).

1) $H_\infty(s)$ is the *open-circuit transfer gain*, which corresponds to the transfer gain $H(s)$ evaluated with the extra element removed, namely the $a-a'$ branch is

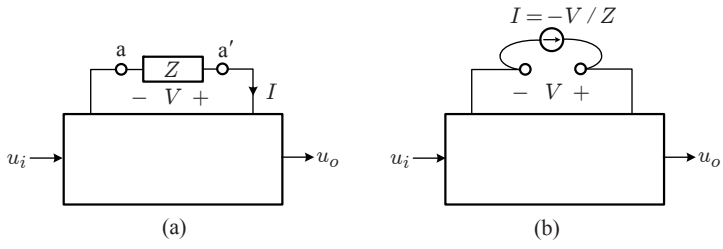


Figure 1.11 Network representations. (a) Original representation. (b) Alternative representation.

open-circuited: $H_\infty(s) = u_o(s)/u_i(s)_{Z(s)=\infty}$. This transfer gain is illustrated in Fig. 1.10(b).

2) $\bar{z}(s)$ is the *driving point impedance*, which represents the input impedance looking into the $a - a'$ branch under the condition that the input of the transfer gain is disabled: $u_i(s) = 0$. Referring to Fig. 1.10(c), this impedance is described as $\bar{z}(s) = V(s)/I(s)_{u_i(s)=0}$

3) $\bar{\zeta}(s)$ represents the *null driving point impedance*, which is the input impedance looking into the $a - a'$ branch under the following specific operational circumstance. Referring to Fig. 1.10(d), the null driving point impedance is evaluated when the output variable $u_o(s)$ is *nullified* by exciting the network with the two specially-selected variables of $u_i'(s)$ and $I'(s)$: i.e., $u_o(s) = 0$ when $u_i(s) = u_i'(s)$ and $I(s) = I'(s)$. In Fig. 1.10(d), the null driving point impedance is defined as $\bar{\zeta}(s) = V'(s)/I'(s)_{u_o(s)=0}$

The EET is a very powerful and versatile means to study transfer functions of complex networks. As one important application, the EET is used to evaluate the transfer function under the circumstance that the transfer gain of the initial network is known and an extra component is added to the network afterwards. For example, the transfer gain of the converter connected to a current sink, thus with the condition $Z(s) = \infty$, is already analyzed in the previous section. Now, the current sink is replaced with a practical load with a certain load impedance, thus $Z(s) \neq \infty$. For this case, we utilize the EET of (1.53) to find the expression for the transfer gain, $H(s)$, in the presence of $Z(s)$. With the known $H_\infty(s)$ and $Z(s)$, we only need to evaluate the driving point impedance $\bar{z}(s)$ and the null driving point impedance $\bar{\zeta}(s)$, which is usually a straightforward process.

Proof of EET

This section provides the proof of the EET. The network representation in Fig. 1.10(a) is repeated in Fig. 1.11(a), where the terminal current $I(s)$ and terminal voltage $V(s)$ are the circuit variables associated with the impedance element $Z(s)$.

The terminal voltage and current of the impedance element are linked by the equation $I(s) = -V(s)/Z(s)$. Figure 1.11(a) is redrawn in Fig. 1.11(b) using this relationship.

By considering $u_i(s)$ and $I(s)$ as the input variables and $u_o(s)$ and $V(s)$ as the output variables, the circuit equations for Fig. 1.11(b) are written as

$$\begin{aligned} u_o(s) &= a_{11}u_i(s) + a_{12}I(s) \\ V(s) &= a_{21}u_i(s) + a_{22}I(s) \end{aligned} \tag{1.54}$$

with

$$V(s) = -I(s)Z(s) \tag{1.55}$$

Referring to the expression (1.54), the coefficient $a_{11} = u_o(s)/u_i(s)_{I(s)=0}$ is the transfer gain evaluated with the condition $Z(s) \to \infty$ (or the branch $a-a'$ is opened) so that $I(s) = 0$. This indicates the coefficient a_{11} is the open-circuit transfer gain cited in (1.53): $a_{11} = H_\infty(s)$. Similarly, the coefficient $a_{22} = V(s)/I(s)_{u_i(s)=0}$ is recognized as the driving point impedance $\bar{z}(s)$ defined in (1.53): $a_{22} = \bar{z}(s)$.

We desire to find the expression for the transfer gain, $H(s) = u_o(s)/u_i(s)$. By solving (1.54) and (1.55) simultaneously, the transfer gain is determined as

$$H(s) = \frac{u_o(s)}{u_i(s)} = a_{11}\frac{1 + \dfrac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}}\dfrac{1}{Z(s)}}{1 + \dfrac{a_{22}}{Z(s)}} \tag{1.56}$$

Now, we evaluate the composite coefficient, $(a_{11}a_{22} - a_{12}a_{21})/a_{11}$, emerging in the numerator of (1.56). For this purpose, we now assume that the two input variables, $u_i(s)$ and $I(s)$, are specially adjusted so that the output variable $u_o(s)$ becomes null, $u_o(s) = 0$. With this operational constraint, the equation (1.54) becomes

$$\begin{aligned} 0 &= a_{11}u_i(s) + a_{12}I(s) \\ V(s) &= a_{21}u_i(s) + a_{22}I(s) \end{aligned} \tag{1.57}$$

Equations (1.57) are solved to yield the following relationship

$$\left.\frac{V(s)}{I(s)}\right|_{u_o(s)=0} = \frac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}} \tag{1.58}$$

which states that *the composite coefficient* $(a_{11}a_{22} - a_{12}a_{21})/a_{11}$ *is actually the null driving point impedance* $\bar{\zeta}(s)$ *cited in* (1.53).

By correlating (1.53) and (1.56) with the knowledge $a_{11} = H_\infty(s)$, $a_{22} = \bar{z}(s)$, and $(a_{11}a_{22} - a_{12}a_{21})/a_{11} = \bar{\zeta}(s)$, the EET in (1.53) becomes self-evident.

Comments on Null Driving Point Impedance: The evaluation of the null driving point impedance $\bar{\zeta}(s)$ may seem difficult. But, in reality, the null driving point impedance is determined very simply and is the easiest transfer function among the transfer functions involved with the EET in (1.53). When evaluating the null driving point impedance, we assume that the network variables are forced to *take* the specific values that produce the *zero* output. This constraint greatly simplifies the analysis, as will be shown in the next section.

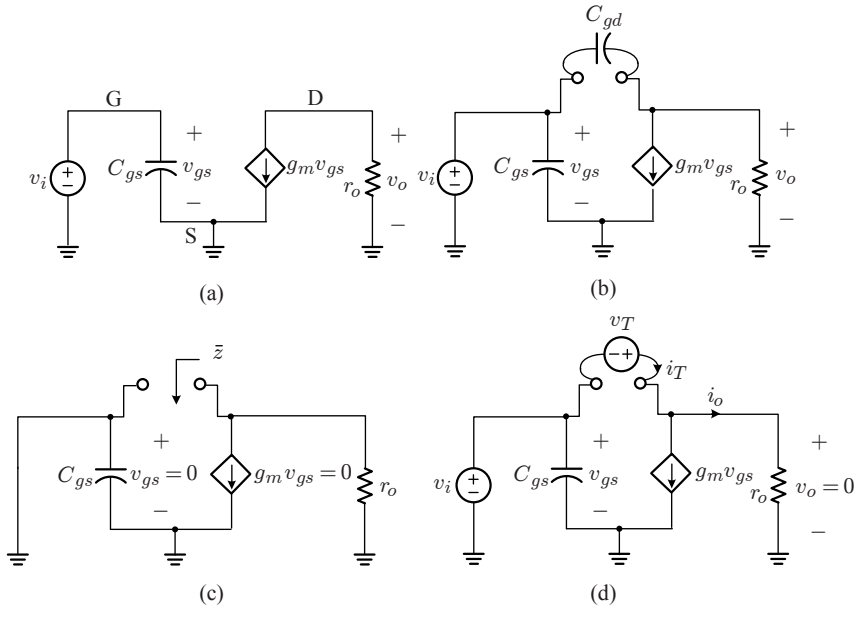


Figure 1.12 Small-signal model of MOSFET amplifier. (a) Small-signal model without C_{gd}. (b) Small-signal model with C_{gd}. (c) Small-signal model for evaluation of $\bar{z}(s)$. (d) Small-signal model for evaluation of $\bar{\zeta}(s)$.

EET Application Example

An easy application of the EET is illustrated using a MOSFET amplifier. Figure 1.12(a) is the small-signal model of a simple MOSFET amplifier, where the parasitic capacitance between the gate and source terminals, C_{gs}, is considered but the gate-drain terminal capacitance is not considered, thus $C_{gd} = 0$ or $1/(sC_{gd}) = \infty$. The input-to-output voltage gain is given as

$$\frac{v_o(s)}{v_i(s)} = -g_m r_o \tag{1.59}$$

Now, the gate-drain terminal capacitance, C_{gd}, is included to the MOSFET. Figure 1.12(b) depicts the small-signal model of the amplifier, where C_{gd} is considered as an extra element. The EET given by (1.53) is invoked to find the voltage gain in the presence of C_{gd}. With the recognition of $v_o(s)/v_i(s)_{Z(s)=\infty} = H_\infty(s) = -g_m r_o$ where $Z(s) = 1/(sC_{gd})$, the expression (1.53) is written as

$$H(s) = \frac{v_o(s)}{v_i(s)}_{Z(s)\neq\infty} = -g_m r_o \frac{1 + sC_{gd}\,\bar{\zeta}(s)}{1 + sC_{gd}\,\bar{z}(s)} \tag{1.60}$$

for the voltage gain of the MOSFET amplifier. Figure 1.12(c) is the small-signal model of the amplifier, modified to derive the driving point impedance, $\bar{z}(s)$, seen by

C_{gd} with $v_i(s) = 0$. The driving point input impedance is given by

$$\bar{z}(s) = r_o \tag{1.61}$$

The derivation of the null driving point impedance is illustrated in Fig. 1.12(d). Here, the condition $v_o(s) = 0$ is obtained by exciting the amplifier with the two specially-selected signals, $v_i(s)$ and $i_T(s)$. The null driving point impedance, $\bar{\zeta}(s)$, is expressed as

$$\bar{\zeta}(s) = \frac{v_T(s)}{i_T(s)}_{v_o(s)=0} \tag{1.62}$$

The condition $v_o(s) = 0$ in Fig. 1.12(d) implies the following two facts

i) $v_o(s) = 0 \quad \Rightarrow \quad i_o = 0 \quad \Rightarrow \quad i_T = g_m v_{gs}$,
ii) $v_o(s) = 0 \quad \Rightarrow \quad v_T = -v_{gs}$

The null driving point impedance is now evaluated as

$$\bar{\zeta}(s) = \frac{v_T(s)}{i_T(s)}_{v_o(s)=0} = \frac{-v_{gs}}{g_m v_{gs}} = -\frac{1}{g_m} \tag{1.63}$$

The expression for the voltage gain in the presence of C_{gd} is determined as

$$H(s) = -g_m r_o \frac{1 - \dfrac{sC_{gd}}{g_m}}{1 + sC_{gd} r_o} \tag{1.64}$$

For this simple example, the $v_i(s)$ and $i_T(s)$ that establish *the output-variable nullifying condition*, $v_o(s) = 0$, can be easily found. When the current source $i_T(s)$ is selected as $i_T(s) = g_m v_i(s)$ for an arbitrary $v_i(s)$, the output current $i_o(s)$ becomes *zero*, thereby forcing the output voltage to be null, $v_o(s) = 0$: namely, $i_T(s) = g_m v_i(s) \rightarrow i_o(s) = 0 \rightarrow v_o(s) = 0$. However, the knowledge of this output-variable nullifying condition is not needed to find the null driving point impedance $\bar{\zeta}(s)$. We just assumed that the output voltage is forced to be zero and exploited this fact to find $\bar{\zeta}(s)$.

Alternative Form of EET

The original EET given by (1.53) can be reformulated into an alternative form

$$\begin{aligned} H(s) = H_\infty(s) \frac{1 + \dfrac{\bar{\zeta}(s)}{Z(s)}}{1 + \dfrac{\bar{z}(s)}{Z(s)}} &= H_\infty(s) \frac{Z(s) + \bar{\zeta}(s)}{Z(s) + \bar{z}(s)} \\ &= H_\infty(s) \frac{\bar{\zeta}(s)}{\bar{z}(s)} \frac{1 + \dfrac{Z(s)}{\bar{\zeta}(s)}}{1 + \dfrac{Z(s)}{\bar{z}(s)}} \end{aligned} \tag{1.65}$$

When the expression (1.65) is evaluated with the extra element shorted so that $Z(s) = 0$, it follows that

$$H(s)_{Z(s)=0} = H_\infty(s)\frac{\bar{\zeta}(s)}{\bar{z}(s)} \tag{1.66}$$

Accordingly, the first term in (1.65) is interpreted as the transfer gain assessed under the condition that the extra element is shorted

$$H_\infty(s)\frac{\bar{\zeta}(s)}{\bar{z}(s)} = H(s)_{Z(s)=0} = H_0(s) \tag{1.67}$$

The alternative EET in (1.65) is rewritten as

$$\boxed{H(s) = H_0(s)\,\frac{1+\dfrac{Z(s)}{\bar{\zeta}(s)}}{1+\dfrac{Z(s)}{\bar{z}(s)}}} \tag{1.68}$$

where $H_0(s)$ is the transfer gain calculated with the extra element shorted.

The alternative EET in (1.68) is also very useful in analyzing the performance of coupled converters. For example, we analyzed the performance of the converter with an ideal voltage source, thus assuming the zero source impedance: $Z(s) = 0$. When the ideal voltage source is replaced with a practical source with a finite output impedance, $Z(s) \neq 0$, the alternative EET in (1.68) can be adopted.

Extension of Extra Element Theorem

The EET can be extended to more complex networks by designating multiple components as extra elements and sequentially applying the EET in a nested manner. Figure 1.13 illustrates the procedures of analyzing a complex network by two consecutive adoptions of the EET. We intend to derive the transfer gain, $H(s) = u_o(s)/u_i(s)$, of the network in Fig. 1.13(a). The two impedance elements in Fig. 1.13(a), $Z_1(s)$ and $Z_2(s)$, are assigned as the extra elements. In reference to Fig. 1.13(a), a *reduced model* in Fig. 1.13(b) is obtained by shorting $Z_1(s)$ and opening $Z_2(s)$: $Z_1(s) = 0$ and $Z_2(s) = \infty$.

The transfer gain of the reduced model is denoted as

$$\left.\frac{u_o(s)}{u_i(s)}\right|_{Z_1(s)=0\ Z_2(s)=\infty} = H_s(s) \tag{1.69}$$

The transfer gain $H_s(s)$ is much easier to evaluate, compared with the original transfer gain.

Next, the reduced model of Fig. 1.13(b) is converted into Fig. 1.13(c) by restoring the impedance element $Z_2(s)$ while keeping $Z_1(s)$ shorted. Referring to (1.53), the

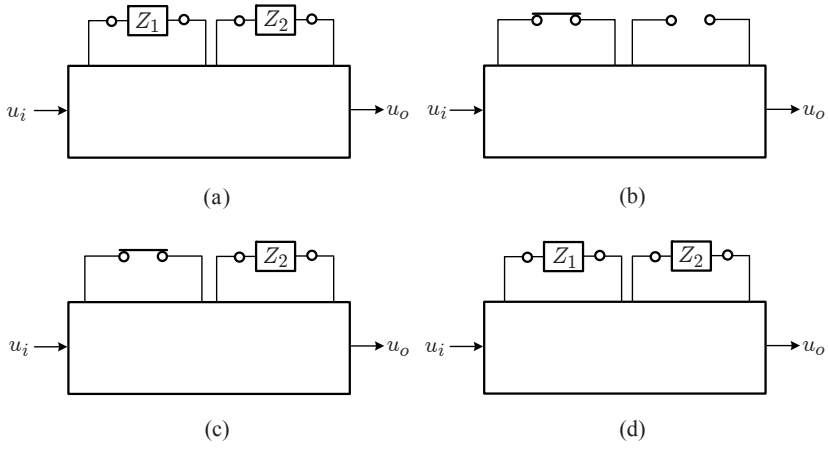


Figure 1.13 Application of EET for two extra elements. (a) Original network. (b) Reduced network. (c) Partially restored network. (d) Fully restored network.

transfer gain of Fig. 1.13(c) is determined as

$$\left.\frac{u_o(s)}{u_i(s)}\right|_{Z_1(s)=0\ Z_2(s)\neq\infty} = H_s(s)\,\frac{1+\dfrac{\bar{\zeta}_2(s)}{Z_2(s)}}{1+\dfrac{\bar{z}_2(s)}{Z_2(s)}} \tag{1.70}$$

where $\bar{\zeta}_2(s)$ is the null driving point impedance seen by $Z_2(s)$ under the condition $Z_1(s)$ is shorted. Similarly, $\bar{z}_2(s)$ is the driving point impedance seen by $Z_2(s)$ with $Z_1(s)$ shorted.

As the last step, the original network is fully restored as shown in Fig. 1.13(d) by reinstating $Z_1(s)$. The EET in (1.68) is now applied to Fig. 1.13(d) to yield

$$\left.\frac{u_o(s)}{u_i(s)}\right|_{Z_1(s)\neq0\ Z_2(s)\neq\infty} = \left(H_s(s)\,\frac{1+\dfrac{\bar{\zeta}_2(s)}{Z_2(s)}}{1+\dfrac{\bar{z}_2(s)}{Z_2(s)}}\right)\left(\frac{1+\dfrac{Z_1(s)}{\bar{\zeta}_1(s)}}{1+\dfrac{Z_1(s)}{\bar{z}_1(s)}}\right) = H(s) \tag{1.71}$$

where $\bar{\zeta}_1(s)$ is the null driving point impedance seen by $Z_1(s)$ when $Z_2(s)$ is present. On the other hand, $\bar{z}_1(s)$ is the driving point impedance seen by $Z_1(s)$ with the same condition.

The final expression of (1.71) is referred to as the 2-EET in the previous publication [3]. The 2-EET can be utilized to investigate the performance of converters, connected to a real source and practical load. We already analyzed the converters operating with an ideal voltage source and current sink load, which corresponds to the reduced network in Fig. 1.13(b). The performance of the uncoupled converters can be transformed to that of the coupled converters, which is represented by the restored network in Fig. 1.13(d), by applying (1.70) and (1.71) in sequence.

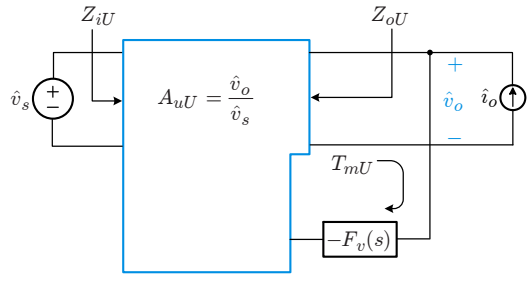


Figure 1.14 Small-signal models of uncoupled converter.

Prolific Feature of EET: The analysis of complex networks can be simplified by designating an impedance component as the extra element and applying the EET. The application of EET will be further extended by assigning multiple impedance components as extra elements. The EET was extended to the 2-EET in this section. This procedure can be repeated to yield an n-EET to deal with n extra elements. This prolific feature of the EET is the distinctive advantage in analyzing dc power conversion systems, where converters and filter stages are first designed as standalone modules and later integrated together to function as an integrated system. The EET provides systematic analysis procedures for otherwise intractable dc power conversion systems.

1.3.2 Performance of Coupled Converter

In the previous section, we studied Middlebrook's extra element theorem as a general network analysis tool. Now, the results of the previous section are adopted to investigate the performance of coupled converters. First, we derive the transfer functions of converters coupled with a practical load. Second, the performance of converters powered by a non-ideal voltage source is analyzed. Lastly, the transfer functions of converters combined with both practical load and non-ideal source are discussed.

Figure 1.14 shows the small-signal model of the uncoupled converter. The subscript $_U$ in the transfer functions signify the uncoupled conditions, $Z_s(s) = 0$ and $Z_L(s) = \infty$. Using Fig. 1.14 as a reference, this section employs the EET to express the performance of coupled converters.

Load-Coupled Converters

The converter coupled with a general load subsystem, but still powered from an ideal voltage source, is denoted as the load-coupled converter. The small-signal block diagram of load-coupled converters is shown in Fig. 1.15(a), where the load impedance $Z_L(s)$ is treated as an extra element. For the application of the EET,

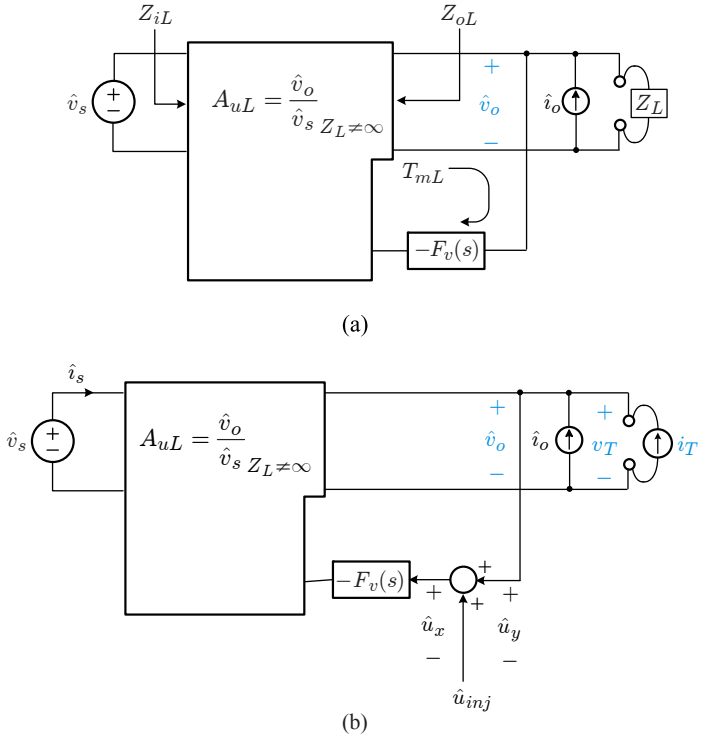


Figure 1.15 Small-signal block diagrams of PWM converter connected to load impedance. (a) Original block diagram. (b) Modified block diagram for EET application.

the block diagram is modified to Fig. 1.15(b). The summing junction in the voltage feedback path is needed for the loop gain analysis.

By applying the EET in (1.53) to Fig. 1.15(b), the audio-susceptibility is expressed as

$$A_{uL}(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)}_{Z_L \neq \infty \; \hat{u}_{inj}=0 \; \hat{i}_o=0} = A_{uU}(s) \frac{1 + \dfrac{\bar{\zeta}'_L(s)}{Z_L(s)}}{1 + \dfrac{\bar{z}'_L(s)}{Z_L(s)}} \tag{1.72}$$

The subscript $_L$ in $A_{uL}(s)$ signifies the presence of the load impedance $Z_L(s)$. The null driving point impedance $\bar{\zeta}'_L(s) = v_T(s)/i_T(s)_{\hat{v}_o=0}$ becomes zero because the null condition $\hat{v}_o(s) = 0$ implies $v_T(s) = 0$: $\bar{\zeta}'_L(s) = 0$. The driving point impedance $\bar{z}'_L(s) = v_T(s)/i_T(s)_{\hat{v}_s=o}$ is the output impedance of the uncoupled converter: $\bar{z}'_L(s) = Z_{oU}(s)$. The final expression of the audio-susceptibility then

becomes

$$\boxed{A_{uL}(s) = A_{uU}(s)\frac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}} \tag{1.73}$$

Similarly, it can be shown that the output impedance of the converter is given by

$$\boxed{Z_{oL}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)}_{Z_L\neq\infty\ \hat{u}_{inj}=0\ \hat{v}_s=0} = Z_{oU}(s)\ \frac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}} \tag{1.74}$$

The input impedance of the converter is expressed as [†]

$$Z_{iL}(s) = \frac{\hat{v}_s(s)}{\hat{i}_s(s)}_{Z_L\neq\infty\ \hat{u}_{inj}=0\ \hat{i}_o=0} = Z_{iU}(s)\ \frac{1+\dfrac{\bar{\zeta}_L''(s)}{Z_L(s)}}{1+\dfrac{\bar{z}_L''(s)}{Z_L(s)}} \tag{1.75}$$

The null driving point impedance $\bar{\zeta}_L''(s) = v_T(s)/i_T(s)_{\hat{v}_s=0}$ is the output impedance of the uncoupled converter: $\bar{\zeta}_L''(s) = Z_{oU}(s)$. On the other hand, the driving point impedance $\bar{z}_L''(s) = v_T(s)/i_T(s)_{\hat{i}_s=0}$ is the output impedance of the uncoupled converter, determined with the input port opened. This driving point impedance is denoted as $Z_o'(s)$. The input impedance is now given by

$$\boxed{Z_{iL}(s) = Z_{iU}(s)\ \frac{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}{1+\dfrac{Z_o'(s)}{Z_L(s)}}} \tag{1.76}$$

For the loop gain evaluation, the signal source $\hat{u}_{inj}(s)$ at the summing junction is activated. The loop gain is defined as

$$T_{mL}(s) = -\frac{\hat{u}_y(s)}{\hat{u}_x(s)}_{Z_L\neq\infty\ \hat{v}_s=0\ \hat{i}_o=0} = T_{mU}(s)\frac{1+\dfrac{\bar{\zeta}_L'''(s)}{Z_L(s)}}{1+\dfrac{\bar{z}_L'''(s)}{Z_L(s)}} \tag{1.77}$$

The null driving point impedance $\bar{\zeta}_L'''(s) = v_T(s)/i_T(s)_{\hat{u}_y=0}$ is zero because the condition $\hat{u}_y(s) = 0$ implies $v_T(s) = 0$. The driving point impedance $\bar{z}'''(s) = v_T(s)/i_T(s)_{\hat{u}_x=0}$ corresponds to the output impedance the uncoupled converter,

[†]Theoretically, the equation should be formulated using the input admittance, $Y_{iL}(s) = 1/Z_{iL}(s) = \hat{i}_s(s)/\hat{v}_s(s)$, because the input variable of dc-to-dc converters is $\hat{v}_s(s)$ not $\hat{i}_s(s)$. However, the formulation using $Y_{iL}(s)$ transforms to (1.75) when the final result is rearranged for $Z_{iL}(s)$.

evaluated with the voltage feedback loop opened. Thus, $\bar{z}_L'''(s)$ becomes the open-loop output impedance of the uncoupled converter.

It is well known that the following relation holds among the open-loop output impedance $\bar{z}_L'''(s)$, closed-loop output impedance $Z_{oU}(s)$, and loop gain $T_{mU}(s)$ of the uncoupled converter

$$Z_{oU}(s) = \frac{\bar{z}_L'''(s)}{1 + T_{mU}(s)} \tag{1.78}$$

which is rearranged as

$$\bar{z}_L'''(s) = Z_{oU}(s)\big(1 + T_{mU}(s)\big) \tag{1.79}$$

By incorporating (1.79) and $\bar{\zeta}_L'''(s) = 0$ into (1.77), the loop gain is expressed as

$$T_{mL}(s) = T_{mU}(s)\,\frac{1}{1 + (1 + T_{mU})\,\dfrac{Z_{oU}(s)}{Z_L(s)}} \tag{1.80}$$

The performance of load-coupled converters can be investigated using the equations (1.73), (1.74), (1.76), and (1.80). Once the load impedance $Z_L(s)$ is available, the performance of the load-coupled converter is predicted by analyzing these equations. Procedures and outcomes of such analyses will be given in the next chapter. The results of this section are summarized in Table 1.1 for easy referencing.

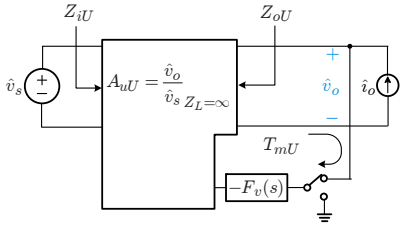
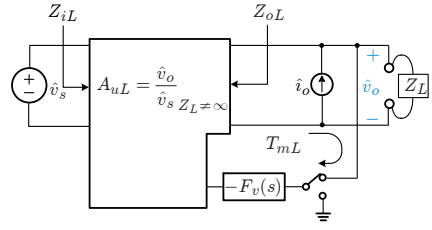
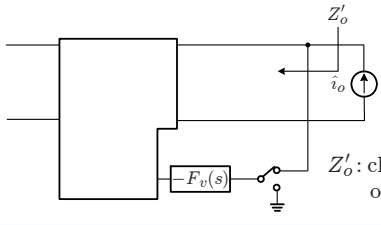
EXAMPLE 1.3 Performance of Load-Coupled Boost Converter

PWM converters are frequently employed in a cascaded structure for an efficient power conversion. For such cases, an intermediate line filter stage is usually employed between the converters. This example illustrates the performance of a current-mode controlled boost converter coupled with a buck converter through a line filter stage. As shown in Fig. 1.16(a), the boost converter provides a 46 V dc for the buck converter. The buck converter then draws a 2 A current from the boost converter via the line filter stage. The boost converter sees the combination of the line filter and buck converter as a load subsystem.

Figure 1.16(b) shows the load impedance $Z_L(s)$ seen by the output of the boost converter. Details about the load impedance will be given in the next chapter. Figures 1.16(c) through 1.16(e) illustrate the audio-susceptibility, output impedance, and loop gain of the load-coupled boost converter, in comparison with those of the converter directly connected to a 2 A current sink, the uncoupled boost converter.

The performance of the load-coupled converter significantly differs from that of the uncoupled converter. Even so, the performance of the load-coupled converter can be closely predicted by applying the graphical analysis to (1.73), (1.74), (1.76), and (1.80). In the next chapter, we will employ the graphical analysis to uncover the behavior of the load-coupled converter.

Table 1.1 Performance of Load-Coupled Converter

Performance expression	
	
Uncoupled converter	Load-coupled converter
$A_{uL}(s)=A_{uU}(s)\dfrac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}$	$Z_{oL}(s)=Z_{oU}(s)\dfrac{1}{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}$
$T_{mL}(s)=T_{mU}(s)\dfrac{1}{1+(1+T_{mU}(s))\dfrac{Z_{oU}(s)}{Z_L(s)}}$	$Z_{iL}(s)=Z_{iU}(s)\dfrac{1+\dfrac{Z_{oU}(s)}{Z_L(s)}}{1+\dfrac{\bar{z}'_o(s)}{Z_L(s)}}$
Output impedance definition	
 Z'_o: closed-loop input-open output impedance	

Source-Coupled Converters

We utilize the EET to study the performance of the converters powered by a non-ideal voltage source. The converter supported by a non-ideal source but connected to a current sink is referred to as the *source-coupled converter*. Figure 1.17(a) is the small-signal block diagram of the source-coupled converter, where the source impedance $Z_s(s)$ is considered as an extra element. The small-signal block diagram is modified to Fig. 1.17(b) for the EET application.

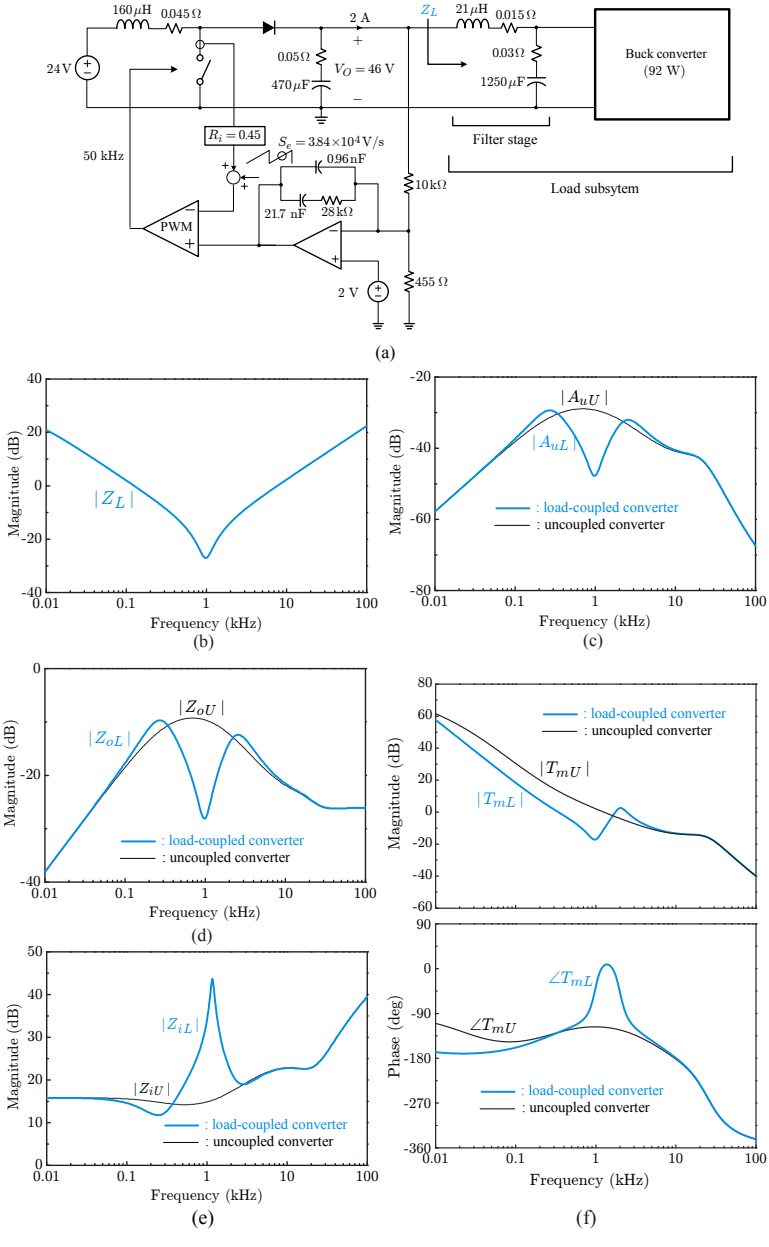


Figure 1.16 Performance of load-coupled and uncoupled boost converters. (a) Boost converter feeding buck converter via filter stage. (b) Load impedance. (c) Audio-susceptibility. (d) Output impedance. (e) Loop gain.

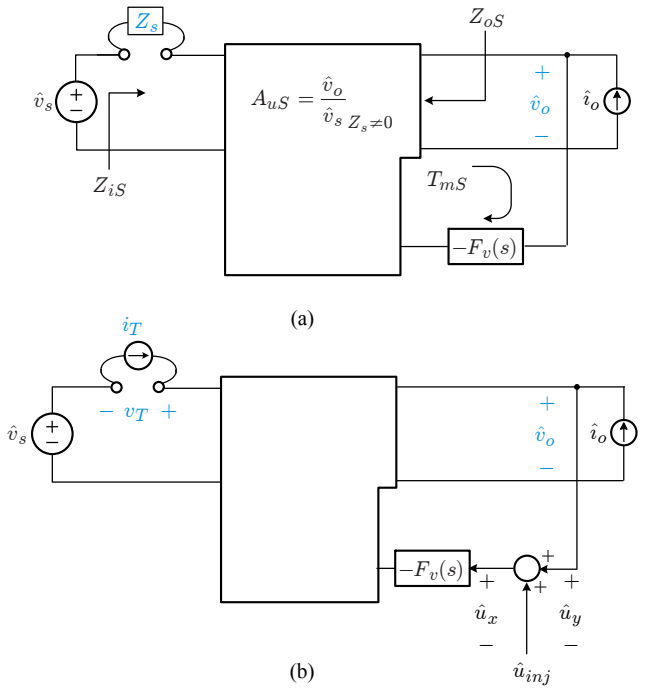


Figure 1.17 Small-signal block diagrams of PWM converter connected to source impedance. (a) Original block diagram. (b) Modified block diagram for EET application.

Using the alternative EET expression in (1.68), the audio-susceptibility is determined as

$$A_{uS}(s) = \frac{\hat{v}_o(s)}{\hat{v}_s(s)}_{Z_s \neq 0\ \hat{u}_{inj}=0\ \hat{i}_o=0} = A_{uU}(s)\ \frac{1 + \dfrac{Z_s(s)}{\bar{\zeta}_s'(s)}}{1 + \dfrac{Z_s(s)}{\bar{z}_s'(s)}} \tag{1.81}$$

where $A_{uU}(s)$ is the audio-susceptibility of the converter connected to an ideal voltage source, or the uncoupled converter. The null driving point impedance $\bar{\zeta}_s'(s) = v_T(s)/i_T(s)_{\hat{v}_o=0}$ becomes infinite for the following reasons.

i) The condition $\hat{v}_o(s) = 0$ with $\hat{v}_s(s) \neq 0$ implies the input signal path is opened.

ii) This condition is identical to $i_T(s) = 0$ which in turn makes $\bar{\zeta}_s'(s) = \infty$.

On the other hand, the driving point impedance $\bar{z}_s'(s) = v_T(s)/i_T(s)_{\hat{v}_s=o}$ is the input impedance of the uncoupled converter: $\bar{z}_s'(s) = Z_{iU}(s)$. The audio-susceptibility is then expressed as

$$\boxed{A_{uS}(s) = A_{uU}(s)\ \frac{1}{1 + \dfrac{Z_s(s)}{Z_{iU}(s)}}} \tag{1.82}$$

The output impedance the converter is given by

$$Z_{oS}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)}_{Z_s\neq 0\ \hat{u}_{inj}=0\ \hat{v}_s=0} = Z_{oU}(s)\ \frac{1+\dfrac{Z_s(s)}{\bar{\zeta}_s''(s)}}{1+\dfrac{Z_s(s)}{\bar{z}_s''(s)}} \tag{1.83}$$

The evaluation of the null driving point impedance $\bar{\zeta}_s''(s) = v_T(s)/i_T(s)_{\ \hat{v}_o=0}$ needs a special attention. The condition $\hat{v}_o(s) = 0$ with $\hat{i}_o(s) \neq 0$ indicates that the output port of the converter is shorted. When the output is shorted, the feedback from the output voltage is disabled. Accordingly, the null driving point impedance $\bar{\zeta}_s''(s)$ is the input impedance of the uncoupled converter, evaluated under the condition that the output port is shorted and the voltage feedback is broken. This input impedance is denoted as $Z_i'(s)$. The driving point impedance $\bar{z}_s''(s) = v_T/i_{T\,\hat{i}_o=o}$ is the input impedance of the uncoupled converter: $\bar{z}_s''(s) = Z_{iU}(s)$. The output impedance is then determined as

$$\boxed{Z_{oS}(s) = Z_{oU}(s)\ \frac{1+\dfrac{Z_s(s)}{Z_i'(s)}}{1+\dfrac{Z_s(s)}{Z_{iU}(s)}}} \tag{1.84}$$

The loop gain of the source-coupled converter is expressed as

$$T_{mS}(s) = -\frac{\hat{u}_y(s)}{\hat{u}_x(s)}_{Z_s\neq 0\ \hat{v}_s=0\ \hat{i}_o=0} = T_{mU}(s)\ \frac{1+\dfrac{Z_s(s)}{\bar{\zeta}_s'''(s)}}{1+\dfrac{Z_s(s)}{\bar{z}_s'''(s)}} \tag{1.85}$$

The null driving point impedance $\bar{\zeta}_s'''(s) = v_T(s)/i_T(s)_{\ \hat{u}_y=0}$ is identified as follows. The condition $\hat{u}_y(s) = 0$ with $\hat{i}_o(s) = 0$, which is identical to the case $\hat{v}_o(s) = 0$ with $\hat{i}_o(s) = 0$, *does not* imply a short circuit situation at the output port. Instead, it indicates that the output is nullified, $\hat{v}_o(s) = 0$, by exciting the converter with a specially-selected $\{\hat{u}_x(s)\,, i_T(s)\}$ pair, while the output voltage feedback is active. Accordingly, the null driving point impedance $\bar{\zeta}_s'''(s) = v_T(s)/i_T(s)_{\ \hat{u}_y=0}$ is interpreted as the input impedance of the converter, determined when the feedback loop is closed but the output voltage is nullified, $\hat{v}_o(s) = 0$. This closed-loop null driving point impedance is denoted as $Z_i''(s)$.

The driving point impedance $\bar{z}_s'''(s) = v_T(s)/i_T(s)_{\ \hat{u}_x=0}$ is interpreted as the input impedance of the converter under the open-loop condition, because $\hat{u}_x(s) = 0$ indicates the output voltage feedback is disabled. This open-loop driving point impedance is represented by $Z_i'''(s)$. The loop gain of the source-coupled converter is expressed as

$$\boxed{T_{mS}(s) = T_{mU}(s)\ \frac{1+\dfrac{Z_s(s)}{Z_i''(s)}}{1+\dfrac{Z_s(s)}{Z_i'''(s)}}} \tag{1.86}$$

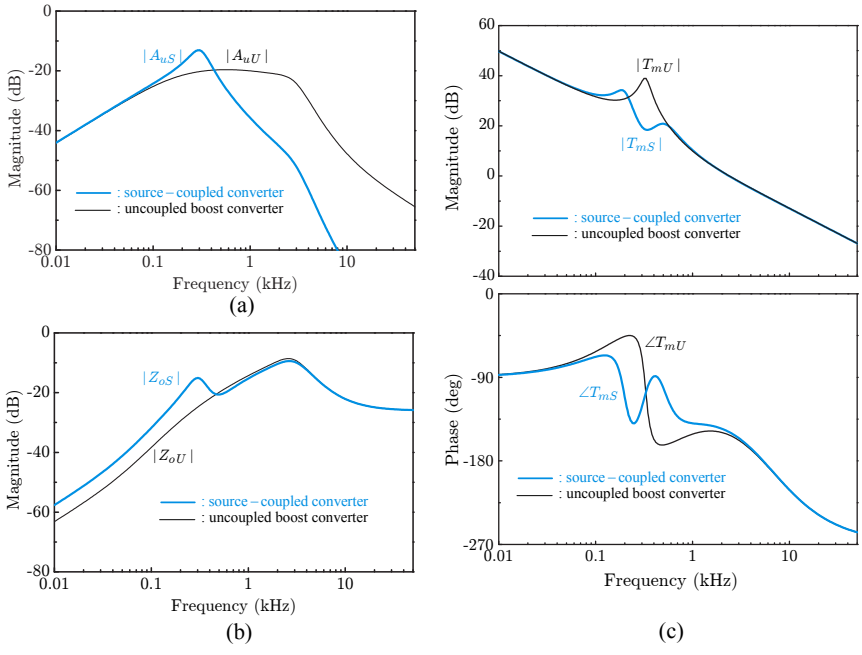


Figure 1.18 Performance of source-coupled and uncoupled boost converters. (a) Output impedance. (b) Loop gain.

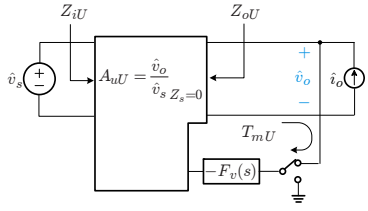
The graphical analysis method can be applied to the equations of (1.82), (1.84), and (1.86), to investigate the closed-loop performance of the source-coupled converter. This topic will be covered in the next chapter. Table 1.2 highlights the results of this section, along with the illustration of the various input impedances of the uncoupled converter, appearing in the transfer functions of the source-coupled converter. The evaluation of these input impedances will also be discussed in the next chapter.

Performance of Source-Coupled Boost Converter EXAMPLE 1.4

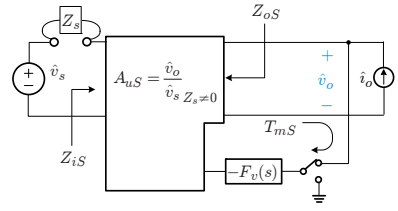
This example demonstrates the performance of a source-coupled boost converter. Shown in Fig. 1.18 are the output impedance and loop gain of the boost converter powered by a practical voltage source with a finite output impedance. The converter performance is compared with that of the uncoupled converter. The source-coupled converter shows significant changes. In the next chapter, we will closely investigate the behavior of the source-coupled converter.

Table 1.2 Performance of Source-Coupled Converter

Performance expression



Uncoupled converter



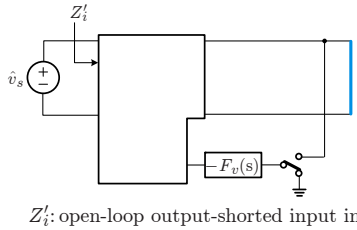
Source-coupled converter

$$A_{uS}(s) = A_{uU}(s)\frac{1}{1+\dfrac{Z_s(s)}{Z_{iU}(s)}}$$

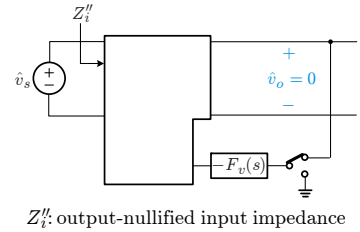
$$Z_{oS}(s) = Z_{oU}(s)\frac{1+\dfrac{Z_s(s)}{Z_i'(s)}}{1+\dfrac{Z_s(s)}{Z_{iU}(s)}}$$

$$T_{mS}(s) = T_{mU}(s)\frac{1+\dfrac{Z_s(s)}{Z_i''(s)}}{1+\dfrac{Z_s(s)}{Z_i'''(s)}}$$

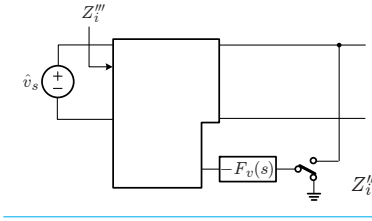
Input impedance definition



Z_i': open-loop output-shorted input impedance



Z_i'': output-nullified input impedance



Z_i''': open-loop input impedance

Source/Load-Coupled Converters

Discussions of the previous sections are extended to the converters combined with both the practical load and non-ideal source. For this purpose, the results of the earlier 2-EET can be adopted. For example, the loop gain of the converter with both

the load impedance $Z_L(s)$ and source impedance $Z_s(s)$ is obtained through the two sequential adoptions of EET. The loop gain with $Z_L(s)$ is given by

$$T_{mL}(s) = T_{mU}(s)\,\frac{1}{1+\big(1+T_{mU}(s)\big)\dfrac{Z_{oU}(s)}{Z_L(s)}} \tag{1.87}$$

by the first EET adoption. When the converter is further connected by a non-ideal source with $Z_s(s)$, the second EET of (1.86) is adopted to yield

$$T_{mC}(s) = \left(T_{mU}(s)\,\frac{1}{1+\big(1+T_{mU}(s)\big)\dfrac{Z_{oU}(s)}{Z_L(s)}}\right)\left(\frac{1+\dfrac{Z_s(s)}{Z_i''(s)}}{1+\dfrac{Z_s(s)}{Z_i'''(s)}}\right) \tag{1.88}$$

where the subscript $_C$ in $T_{mC}(s)$ indicates that the converter is fully coupled with both $Z_L(s)$ and $Z_s(s)$. Here, $Z_i''(s)$ *and* $Z_i'''(s)$ *are evaluated under the condition that the load impedance* $Z_L(s)$ *is present*. Although the expression of the loop gain is very involved, the analysis will be facilitated when the graphical analysis method is employed. The above procedure is also applicable to the other performance metrics.

The results of this section will be used in the next chapter to investigate the performance of converters coupled with both real source and load subsystems.

1.3.3 EET Adapted to Feedback-Controlled Systems

In the previous sections, we employed the EET to account for the impacts of an impedance element which was not considered in the initial analysis. We now modify the EET into an alternative format which greatly simplifies the analysis of complex feedback-controlled systems. The modified EET will be used later to evaluate the input impedance of closed-loop controlled converters, whose knowledge is critically needed for the analysis of dc power conversion systems.

The input impedance analysis using the conventional techniques is too complicate to provide any useful data. The modified EET, known as Middlebrook's *feedback theorem*, greatly expedites the analysis and provides valuable information about the input impedance. We first present Middlebrook's feedback theorem and later illustrate its application to the input impedance analysis of closed-loop controlled converters.

EET for Feedback-Controlled Systems

Figure 1.19 shows a feedback-controlled system. The system has two input variables, $u_{i1}(s)$ and $u_{i2}(s)$, and two output variables, $u_{o1}(s)$ and $u_{o2}(s)$. The output variable $u_{o2}(s)$ is multiplied by the feedback gain $A(s)$ and the resulting signal is employed

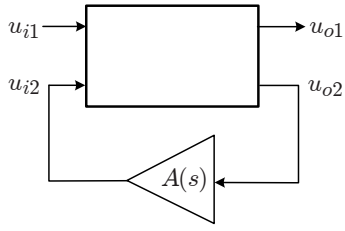


Figure 1.19 Two-output feedback controlled system.

as the input variable $u_{i2}(s)$. The system thus constitutes a two-output feedback-controlled system.

The relationships between the input and output variables are written as

$$\begin{aligned} u_{o1}(s) &= a_{11}u_{i1}(s) + a_{12}u_{i2}(s) \\ u_{o2}(s) &= a_{21}u_{i1}(s) + a_{22}u_{i2}(s) \\ u_{i2}(s) &= A(s)u_{o2}(s) \end{aligned} \tag{1.89}$$

By solving the three equations, the transfer gain from $u_{i1}(s)$ to $u_{o1}(s)$ is determined as

$$H(s) = \frac{u_{o1}(s)}{u_{i1}(s)} = a_{11}\frac{1 + \left(-\dfrac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}}\right)A(s)}{1 + (-a_{22})A(s)} \tag{1.90}$$

Referring to (1.89), the coefficient a_{11} is interpreted as

$$a_{11} = \left.\frac{u_{o1}(s)}{u_{i1}(s)}\right|_{u_{i2}=Au_{o2}=0} \quad \Rightarrow \quad a_{11} = \left.\frac{u_{o1}(s)}{u_{i1}(s)}\right|_{A=0} \equiv H_0(s) \tag{1.91}$$

where $H_0(s)$ represents the transfer gain, evaluated with the condition that the feedback gain is reduced to zero. From (1.89), the coefficient $-a_{22}$ is evaluated as

$$-a_{22} = \left.-\frac{u_{o2}(s)}{u_{i2}(s)}\right|_{u_{i1}=0} \equiv \bar{a}(s) \tag{1.92}$$

where $\bar{a}(s)$ denotes the *(negative) forward gain* of the system evaluated with $u_{i1}(s) = 0$.

By solving (1.89) under the condition $u_{o1}(s) = 0$, the following relation yields

$$\left.-\frac{u_{o2}(s)}{u_{i2}(s)}\right|_{u_{o1}=0} = -\frac{a_{11}a_{22} - a_{12}a_{21}}{a_{11}} \equiv \bar{\alpha}(s) \tag{1.93}$$

The transfer function $\bar{\alpha}(s)$ is referred to as the *(negative) null forward gain*, determined with $u_{o1}(s) = 0$.

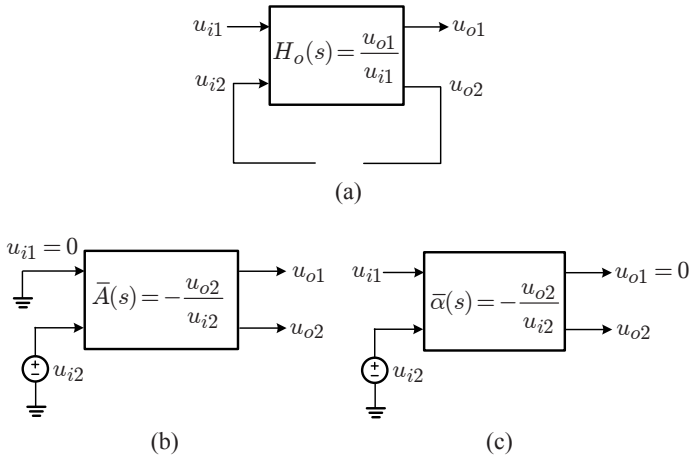


Figure 1.20 Illustration of $H_o(s)$, $\bar{a}(s)$, and $\bar{\alpha}(s)$.

From the above discussions, the transfer gain from $u_{i1}(s)$ to $u_{o1}(s)$ is expressed as

$$H(s)=\frac{u_{o1}(s)}{u_{i1}(s)}=H_0(s)\frac{1+A(s)\bar{\alpha}(s)}{1+A(s)\bar{a}(s)} \tag{1.94}$$

The transfer functions $H_0(s)$, $\bar{a}(s)$, and $\bar{\alpha}(s)$ are pictorially illustrated in Fig. 1.20.

Middlebrook's Feedback Theorem

The EET is further transformed into another format. The transfer gain expression (1.94) is rearranged into an alternative form

$$\begin{aligned} H(s)=H_0(s)\frac{1+A(s)\bar{\alpha}(s)}{1+A(s)\bar{a}(s)} &= H_0(s)\frac{A(s)\bar{\alpha}(s)}{A(s)\bar{a}(s)}\frac{1+\dfrac{1}{A(s)\bar{\alpha}(s)}}{1+\dfrac{1}{A(s)\bar{a}(s)}} \\ &= H_0(s)\frac{\bar{\alpha}(s)}{\bar{a}(s)}\frac{1+\dfrac{1}{A(s)\bar{\alpha}(s)}}{1+\dfrac{1}{A(s)\bar{a}(s)}} \end{aligned} \tag{1.95}$$

When the expression (1.95) is evaluated with the condition $A(s)=\infty$, it follows that

$$H(s)_{A=\infty}=H_0(s)\frac{\bar{\alpha}(s)}{\bar{a}(s)}\equiv H_\infty(s) \tag{1.96}$$

Accordingly, the leading transfer function in (1.95) is identified as the transfer gain assessed under the condition that the feedback gain is infinite. The EET in (1.95) is

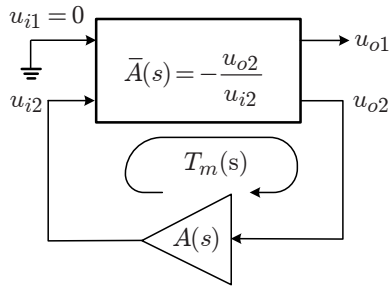


Figure 1.21 Loop gain of two-output feedback-controlled system

now written as

$$H(s) = H_\infty(s)\frac{1+\dfrac{1}{A(s)\bar{\alpha}(s)}}{1+\dfrac{1}{A(s)\bar{a}(s)}} \tag{1.97}$$

where $H_\infty(s)$ is the transfer gain evaluated with $A(s)=\infty$.

The expression (1.97) is further modified into

$$\begin{aligned} H(s) &= H_\infty(s)\frac{1+\dfrac{1}{A(s)\bar{\alpha}(s)}}{1+\dfrac{1}{A(s)\bar{a}(s)}} \\ &= H_\infty(s)\frac{1}{1+\dfrac{1}{A(s)\bar{a}(s)}} + H_\infty(s)\frac{\dfrac{1}{A(s)\bar{\alpha}(s)}}{1+\dfrac{1}{A(s)\bar{a}(s)}} \\ &= H_\infty(s)\frac{A(s)\bar{a}(s)}{1+A(s)\bar{a}(s)} + H_\infty(s)\frac{\bar{a}(s)}{\bar{\alpha}(s)}\frac{1}{1+A(s)\bar{a}(s)} \end{aligned} \tag{1.98}$$

By evaluating (1.98) with the condition $A(s)=0$

$$H(s)_{A=0} = H_\infty(s)\frac{\bar{a}(s)}{\bar{\alpha}(s)} \equiv H_0(s) \tag{1.99}$$

the leading transfer function of the second term in (1.98) is found as the open-loop transfer gain, evaluated with $A(s)=0$.

The term $A(s)\bar{a}(s)$ in (1.98) has a very special implication. The $A(s)\bar{a}(s)$ product

$$A(s)\bar{a}(s) = \frac{u_{i2}(s)}{u_{o2}(s)}(-)\frac{u_{o2}(s)}{u_{i2}(s)} \equiv T_m(s) \tag{1.100}$$

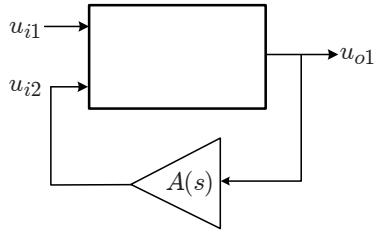


Figure 1.22 Single-output feedback-controlled system

is the loop gain $T_m(s)$ associated with the feedback path,† evaluate with $u_{i1}(s) = 0$. Figure 1.21 is the illustration of the loop gain expression of (1.100).

The final modification of (1.98) is given by

$$H(s) = \frac{u_{o1}(s)}{u_{i1}(s)} = H_\infty(s)\frac{T_m(s)}{1+T_m(s)} + H_0(s)\frac{1}{1+T_m(s)} \tag{1.101}$$

This EET is formulated by R.D. Middlebrook and known as *Middlebrook's feedback theorem*. The transfer functions appearing in the feedback theorem have the following implications.

1) $H_\infty(s)$ is the transfer gain evaluated under the condition that the gain of feedback block is infinite, $A(s) = \infty$. When a normal operation is presumed in Fig. 1.19 with $A(s) = \infty$, the output variable $u_{o2}(s)$ should be zero, in order to force the output of the feedback block, $u_{i2}(s)$, to have a finite value. *This indicates that $H_\infty(s)$ is the transfer gain, determined under the condition that the output variable $u_{o2}(s)$ is nullified.* The evaluation of $H_\infty(s)$ becomes straightforward when the output-variable nullifying condition is exploited.

2) $H_0(s)$ is the transfer gain evaluated with $A(s) = 0$. This transfer gain can readily be assessed by opening the feedback loop linked to $A(s)$.

3) $T_m(s) = A(s)\bar{a}(s)$ is the loop gain associated with the feedback path. The loop gain is usually controlled by the feedback gain $A(s)$ to have a desired structure. Thus, the loop gain characteristics are commonly known in advance. Further details about the loop gain will be given in the next chapter.

The feedback theorem offers a very powerful alternative approach to analyzing feedback-controlled systems. The use of the feedback theorem is illustrated in the next two examples.

†The loop gain was defined as the *negative* gain product of the feedback path.

EXAMPLE 1.5 Feedback Theorem for Single-Output Feedback System

Figure 1.22 shows a single-output feedback-controlled system, where the sole output variable $u_{o1}(s)$ is used as the feedback signal. For this system, $H_\infty(s) = u_{o1}(s)/u_{i1}(s)_{A=\infty}$ is zero, because $u_{o1}(s)$ must be zero in order to produce a finite $u_{i2}(s)$ with the condition $A(s) = \infty$. Thus, the expression (1.101) reduces to

$$H(s) = \frac{u_{o1}(s)}{u_{i1}(s)} = \frac{H_0(s)}{1 + T_m(s)} \tag{1.102}$$

which is the familiar closed-loop transfer gain expression for the single-output system.

EXAMPLE 1.6 Input Impedance of Uncoupled Converter

This example illustrates the use of the feedback theorem to analyze the input impedance of uncoupled converters. Figure 1.23 is the block diagram of the uncoupled converter, modified for the input impedance analysis. Application of the feedback theorem to Fig. 1.23 yields †

$$\frac{1}{Z_{iU}(s)} = \frac{i_T(s)}{v_T(s)} = \frac{1}{Z_i''(s)} \frac{T_{mU}(s)}{1 + T_{mU}(s)} + \frac{1}{Z_i'''(s)} \frac{1}{1 + T_{mU}(s)} \tag{1.103}$$

where $Z_i''(s)$ is the input impedance evaluated with the output voltage nullified and $Z_i'''(s)$ is the open-loop input impedance of the uncoupled converter. The loop gain $T_{mU}(s)$ is defined with $v_T(s) = 0$.

The above equation is approximated as

$$Z_{iU}(s) \approx \begin{cases} Z_i''(s) : \text{for frequencies where } |T_{mU}| \gg 1 \\ Z_i'''(s) : \text{for frequencies where } |T_{mU}| \ll 1 \end{cases} \tag{1.104}$$

to predict the asymptotic behavior of the input impedance. The borderline of the approximation is the 0 dB crossover frequency of the loop gain $T_{mU}(s)$. Thus, the input impedance follows the output-nullified input impedance, $Z_i''(s)$, up to the loop gain crossover frequency and tracks the open-loop input impedance, $Z_i'''(s)$, thereafter.

The previous two examples are very simple applications of Middlebrook's feedback theorem. The true value of the theorem lies in the analysis of the feedback amplifiers and other closed-loop controlled system. Extensive application examples of the theorem are given in [3].

†The expression is written for the inverse of the input impedance, or input admittance, because the input variable of a converter is the voltage source $v_T(s)$ and the output variable is the current flow $i_T(s)$.

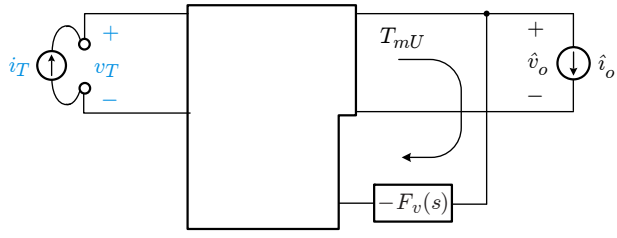


Figure 1.23 Evaluation of input impedance of uncoupled converter.

1.4 CHAPTER SUMMARY

For general dc power conversion applications, individual converters should be designed, fabricated, and tested, as a standalone module at the absence of any knowledge about their source and load subsystems. Under this circumstance, two major challenges exist in the design and analysis of dc-to-dc converters. First, the control design should be executed in the manner that does not call for the source and load impedances while offering good performance for individual converters. The second task is the performance evaluation of the converters integrated with the source and load subsystems whose impedance characteristics are only known afterwards.

To cope with uncertainties in the source and load subsystems, the concept of the uncoupled converter was used. The uncoupled converter is defined as an isolated converter, powered by an ideal voltage source and loaded with current sink. Then, the control design for uncoupled converters is formulated in order to offer good performance when merged with the practical source and load subsystems.

We revealed that the control design for uncoupled converters is the same as the control design intended for a resistive load. This assures that the conventional control design for a resistive load is a correct design approach even though the converter is not connected to a resistor. Furthermore, we demonstrated that the control design is practically not affected by the load impedance, and therefore the standard control design procedures, established for a resistive load in Part I of this book, can be universally applied for all cases.

Middlebrook's extra element theorem (EET) is employed as an instrumental tool to deal with the task of analyzing converters coupled with source and load subsystems. By considering the source impedance and load impedance as the extra elements, the equations of the EET are adopted. The performance of coupled converters is then expressed as the combinations of transfer functions of uncoupled converters, source impedance, and load impedance. The outcomes of this study are summarized in Tables 1.1 and 1.2. This chapter also introduced Middlebrook's feedback theorem, which will be later used in evaluating the input impedance of coupled and uncoupled converters. The next chapter presents comprehensive dynamic analyses of converters coupled with practical source and load subsystem.

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